



General Description

The ISO1540DR devices are low-power bidirectional isolators compatible with the I²C interface. These devices have logic input and output buffers that are separated by using a silicon dioxide (SiO₂) barrier. These devices block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference, and damaging sensitive components.

The ISO1540DR device is based on iDivider® technology with functional, performance, size, and power consumption advantages as compared to optocouplers.

The ISO1540DR provide two bidirectional channels, supporting a complete isolated I²C interface. The ISO1540DR is used in applications that have a single master. This device feature independent 3.0V supplies on each side of the isolator. These devices operate from DC to 2MHz at ambient temperatures of -40°C to +125°C

Features

- Bidirectional I²C communication
- Ultra-low power consumption
- Supports up to 2MHz operation
- Open-drain interfaces
 - Side 1 outputs with 3.5mA sink current
 - Side 2 outputs with 35mA sink current
- 3.0V to 5.5V supply/logic levels
- High common-mode transient immunity: 120kV/μs
- typical RoHS-compliant, SOP-8

Applications

- Isolated I²C, SMBus, PMBus
- interfaces Multilevel I²C interfaces
- Electric and Hybrid-Electric
- Vehicles Open-Drain Networks
- I²C Level Shifting
- Power supplies

Ordering Guide

Table 1. Ordering guide

Model Name ¹	Temperature Range	Total signal channel amount	No. of Bi-directional channels	Isolation Rating (kV rms)	Package	MSL Peak Temp ²	Quantity per reel
ISO1540DR	-40 ~125°C	2	2	3	SOP-8	Level-2-260C-1 YEAR	4000

¹. Pai2xxxxx is equals to π2xxxxx in the customer BOM. Devices with Q suffix are AEC-Q100 qualified.

². MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Functional Block Diagrams

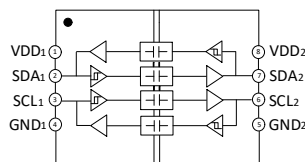


Figure 1. Functional Block Diagram

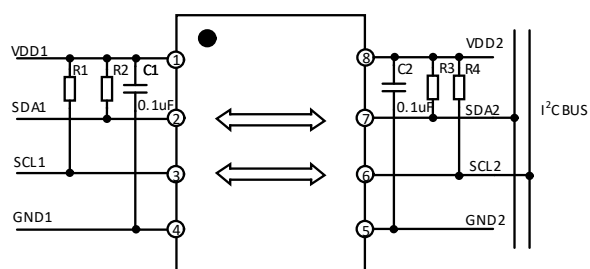
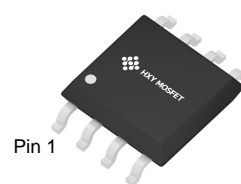


Figure 2. Typical Application Circuit





Pin Configurations And Functions

Table 2. Pin Function Descriptions

Pin No.	Name	Description
1	V _{DD1}	Supply Voltage for Isolator Side 1.
2	SDA ₁	Serial data input / output, side 1.
3	SCL ₁	Serial clock input / output, side 1.
4	GND ₁	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND ₂	Ground 2. This pin is the ground reference for Isolator Side 2.
6	SCL ₂	Serial clock input / output, side 2.
7	SDA ₂	Serial data input / output, side 2.
8	V _{DD2}	Supply Voltage for Isolator Side 2.

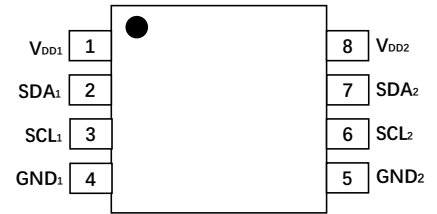


Figure 3. Pin Configuration

Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings⁴

Parameter	Rating
Supply Voltages (V _{DD1} -GND ₁ , V _{DD2} -GND ₂)	-0.5 V to +7.0 V
Signal Voltage SDA1/SCL1	-0.5 V to V _{DDx} + 0.5 V
Signal Voltage SDA2/SCL2	-0.5 V to V _{DDx} + 0.5 V
Average Output Current SDA1/SCL1 (I _{O1})	-20 mA to +20 mA
Average Output Current SDA2/SCL2 (I _{O2})	-100 mA to +100 mA
Storage Temperature (T _{ST}) Range	-65°C to +150°C
Maximum junction temperature T _{J(MAX)}	+150°C

Notes:

1. All voltage values here within are with respect to the local ground pin (GND₁ or GND₂) and are peak voltage values.
2. Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DDx} ¹	3		5.5	V
Input/Output Signal Voltage (V _{SDA1} , V _{SCL1} , V _{SDA2} , V _{SCL2})		0		V _{DDx} ¹	V
Low-level input voltage, side 1	V _{IL1}	0		0.47	V
High-level input voltage, side 1	V _{IH1}	0.7*V _{DD1}		V _{DD1}	V
Low-level input voltage, side 2	V _{IL2}	0		0.3*V _{DD2}	V
High-level input voltage, side 2	V _{IH2}	0.7*V _{DD2}		V _{DD2}	V
Output current, side 1	I _{OL1}	0.5		3.5	mA
Output current, side 2	I _{OL2}	0.5		35	mA
Capacitive load, side 1	C1			40	pF
Capacitive load, side 2	C2			400	pF
Operating frequency	f _{MAX}			2	MHz
Ambient Operating Temperature	T _A	-40		125	°C

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.



Truth Tables

Table 5. Truth Table

V _{ix} Input ¹	V _{DDi} State ¹	V _{DDO} State ¹	V _{Ox} Output ¹
Low	Powered ²	Powered ²	Low
High	Powered ²	Powered ²	High Impedance
Open ⁴	Powered ²	Powered ²	High Impedance
Don't Care	Unpowered ³	Powered ²	High Impedance
Don't Care	Powered ²	Unpowered ³	High Impedance

Notes:

¹ V_{ix}/V_{Ox} are the input/output signals of a given channel (SDA or SCL). V_{DDi}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel. ² Powered means V_{DDx} ≥ 2.95V

³ Unpowered means V_{DDx} < 2.30V

⁴ Invalid input condition as an I²C system requires that a pullup resistor to V_{DD} is connected.

Specifications

Electrical Characteristics

Table 6. DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.0V ~ 5.5V, typical value is measured at T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Side 1 Logic Levels						
Voltage input threshold low, SDA ₁ and SCL ₁	V _{ILT1}	470	510	570	mV	
Voltage input threshold high, SDA ₁ and SCL ₁	V _{IHT1}	540	580	630	mV	
Voltage input hysteresis	V _{HYST1}	30	70		mV	V _{IHT1} - V _{ILT1}
Low-level output voltage, SDA ₁ and SCL ₁	V _{OL1}	650	720	800	mV	0.5 mA ≤ (I _{SDA1} and I _{SCL1}) ≤ 3.5 mA
Low-level output voltage to high-level input voltage threshold difference, SDA ₁ and SCL ₁	ΔV _{OIT1} ¹	60	120		mV	0.5 mA ≤ (I _{SDA1} and I _{SCL1}) ≤ 3.5 mA
Side 2 Logic Levels						
Voltage input threshold low, SDA ₂ and SCL ₂	V _{ILT2}	0.30* V _{DD2}		0.42*V _{DD2}	V	
Voltage input threshold high, SDA ₂ and SCL ₂	V _{IHT2}	0.58* V _{DD2}		0.69*V _{DD2}	V	
Voltage input hysteresis	V _{HYST2}	0.15* V _{DD2}	0.28* V _{DD2}		V	V _{IHT2} - V _{ILT2}
Low-level output voltage, SDA ₂ and SCL ₂	V _{OL2}			0.4	V	0.5 mA ≤ (I _{SDA2} and I _{SCL2}) ≤ 35 mA
Both Sides						
Input leakage currents, SDA ₁ , SCL ₁ , SDA ₂ , and SCL ₂	I _{IN}		0.01	10	μA	V _{SDA1} , V _{SCL1} = V _{DD1} ; V _{SDA2} , V _{SCL2} = V _{DD2}
V _{DDx} ³ Undervoltage Rising Threshold	V _{DDxUV+}	2.45	2.75	2.95	V	
V _{DDx} ³ Undervoltage Falling Threshold	V _{DDxUV-}	2.30	2.60	2.80	V	
V _{DDx} ³ Hysteresis	V _{DDxUVH}		0.15		V	

Notes:

1. ΔV_{OIT1} = V_{OL1} - V_{IHT1}. This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.

2. V_{DDx} is the side voltage power supply VDD, where x = 1 or 2.



Table 7. Quiescent Supply Current

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.0V \sim 5.5V$, typical value is measured at $T_A = 25^\circ C$, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
ISO1540DR	$I_{DD1}(Q)$		1.7	2.4	mA	5V _{DC}	All IO = 0V _{DC}
	$I_{DD2}(Q)$		1.4	2.1	mA		
	$I_{DD1}(Q)$		1.5	2.3	mA		All IO = 5V _{DC}
	$I_{DD2}(Q)$		1.2	1.8	mA		
	$I_{DD1}(Q)$		1.5	2.3	mA	3.3V _{DC}	All IO = 0V _{DC}
	$I_{DD2}(Q)$		1.2	1.8	mA		
	$I_{DD1}(Q)$		1.5	2.3	mA		All IO = 3.3V _{DC}
	$I_{DD2}(Q)$		1.2	1.8	mA		

Table 8. Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.0V \sim 5.5V$, typical value is measured at $T_A = 25^\circ C$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Signal Fall Time SDA1, SCL1	t_{f1}	10	18	32	ns	0.9 × V _{DD1} to 0.9V; R1 = 1500Ω, C1 = 40pF, @ 5V _{DC} supply
		8	16	30	ns	R1 = 1000Ω, C1 = 40pF; @ 3.3V _{DC} supply
Output Signal Fall Time SDA2, SCL2	t_{f2}	20	36	60	ns	0.9 × V _{DD2} to 0.4V; R2 = 150Ω, C2 = 400pF, @ 5V _{DC} supply
		18	31	57	ns	R2 = 100Ω, C2 = 400pF; @ 3.3V _{DC} supply
Low-to-High Propagation Delay, Side 1 to Side 2	t_{pLH1-2}		45	68	ns	0.55V to 0.7 × V _{DD2} ; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10 pF; @ 5V _{DC} supply
			38	63	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ 3.3V _{DC} supply
High-to-Low Propagation Delay, Side 1 to Side 2	t_{pHL1-2}		67	130	ns	0.7V to 0.4V; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ 5V _{DC} supply
			64	130	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ 3.3V _{DC} supply
Pulse Width Distortion [$t_{pHL1-2} - t_{pLH1-2}$]	PWD1-2		22	60	ns	R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ 5V _{DC} supply
			26	65	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ 3.3V _{DC} supply
Low-to-High Propagation Delay, Side 2 to Side 1	t_{pLH2-1}		62	80	ns	0.4 × V _{DD2} to 0.7 × V _{DD1} ; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ 5V _{DC} supply
			50	70	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ 3.3V _{DC} supply
High-to-Low Propagation Delay, Side 2 to Side 1	t_{pHL2-1}		54	84	ns	0.4 × V _{DD2} to 0.9V; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10pF; @ 5V _{DC} supply
			56	86	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10pF; @ 3.3V _{DC} supply
Pulse Width Distortion [$t_{pHL2-1} - t_{pLH2-1}$]	PWD2-1		12	25	ns	R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10 pF; @ 5V _{DC} supply
			15	35	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10 pF; @ 3.3V _{DC} supply
Round-trip propagation delay on Side 1	t_{LOOP1}		116	180	ns	0.4 V to 0.3 × V _{DD1} ; R1 = 1500Ω, R2 = 150Ω, C1, C2 = 10 pF; @ 5V _{DC} supply
			98	162	ns	R1 = 1000Ω, R2 = 100Ω, C1, C2 = 10 pF; @ 3.3V _{DC} supply
Common-Mode Transient Immunity ²	CMTI		120		kV/μs	V _{IN} = V _{DDX} ¹ or 0V, V _{CM} = 1000 V.
ESD (HBM - Human body model)	ESD		±6		kV	



Insulation And Safety Related Specifications

Table 9. Insulation Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage	V _{ISO}	3000	V _{RMS}	1-minute duration, certificated
Minimum External Air Gap (Clearance)	CLR	≥4.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	CRP	≥4.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)	DTI	≥21	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	≥400	V	DIN EN 60112 (VDE 0303-11):2010-05
Material Group		II		IEC 60112:2003 + A1:2009

Package Characteristics

Table 10. Package Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Resistance (Input to Output) ¹	R _{I-O}	≥10 ¹²	Ω	V _{IO} =500V, T _A = 25°C
Resistance (Input to Output) ¹	R _{I-O}	≥10 ¹¹	Ω	V _{IO} =500V, T _A = 125°C
Resistance (Input to Output) ¹	R _{I-O}	≥10 ⁹	Ω	V _{IO} =500V, T _A = 150°C
Capacitance (Input to Output) ¹	C _{I-O}	1.5	pF	@300kHz
Input Capacitance ²	C _I	3	pF	@1MHz, ensured by design
IC Junction to Ambient Thermal Resistance	θ _{JA}	100	°C/W	

Notes:

1. The device is considered a 2-terminal device. Short-circuit all terminals on the VDD₁ side as one terminal and short-circuit all terminals on the VDD₂ side as the other terminal.
2. Testing from the input signal pin to ground.



DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 Insulation Characteristics

Table 11.VDE Insulation Characteristics

Description		Test Conditions/ Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150 V_{RMS}$				I to IV	
For Rated Mains Voltage $\leq 300 V_{RMS}$				I to III	
For Rated Mains Voltage $\leq 400 V_{RMS}$				I to III	
Climatic Classification				40/125/21	
Pollution Degree per DIN VDE 0110, Table 1				2	
Maximum repetitive peak isolation voltage		Time dependent dielectric breakdown test	V_{IORM}	707	V_{peak}
Maximum isolation working voltage		AC voltage (sine wave) DC Voltage	V_{IOWM}	500	V_{RMS}
				707	V_{peak}
	Input to Output Test Voltage, Method B1				
100% production test, no pre-condition tests		$V_{IORM} \times 1.5 = V_{pd(m)}, t_{ini} = t_m = 1 \text{ sec},$ partial discharge $< 5pC$	$V_{pd(m)}$	1061	V_{peak}
	Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1		$V_{IORM} \times 1.3 = V_{pd(m)}, t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec},$ partial discharge $< 5pC$	$V_{pd(m)}$	919	V_{peak}
After Input and/or Safety Test Subgroup 2 and Subgroup 3		$V_{IORM} \times 1.2 = V_{pd(m)}, t_{ini} = 60 \text{ sec}, t_m = 10 \text{ sec},$ partial discharge $< 5pC$	$V_{pd(m)}$	848	V_{peak}
Highest Allowable Overvoltage		$V_{TEST} = V_{IOTM}$ $t = 60s$ (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ $t = 1s$ (100% production)	V_{IOTM}	4200	V_{peak}
Maximum Surge Isolation Voltage		Basic insulation, 1.2/50 μs combination wave, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) ¹	V_{IOSM}	5000	V_{peak}
Safety Limiting Values		Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Safety Temperature			T_S	150	$^{\circ}C$
Maximum Power Dissipation at 25 $^{\circ}C$			P_S	1.25	W
Insulation Resistance		$V_{IO} = 500V, T_A = 25^{\circ}C$	R_{I-O}	$\geq 10^{12}$	Ω
Insulation Resistance		$V_{IO} = 500V,$ $100^{\circ}C \leq T_A \leq 125^{\circ}C$	R_{I-O}	$\geq 10^{11}$	Ω
Insulation Resistance at T_S		$V_{IO} = 500V, T_S = 150^{\circ}C$	R_{I-O}	$\geq 10^9$	Ω

Notes:

¹In accordance with DIN V VDE V 0884-17, ISO1540DR is proof tested by applying a surge isolation voltage of 6500V.



Typical Thermal Characteristics

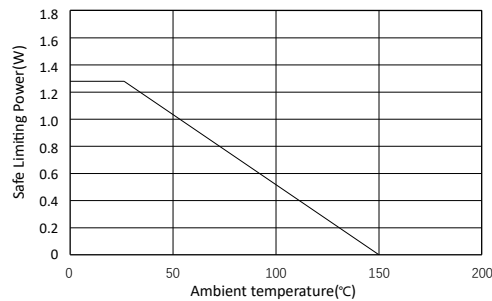


Figure 4. Thermal Derating Curve, Dependence Of Safety Limiting Values with Ambient Temperature per VDE

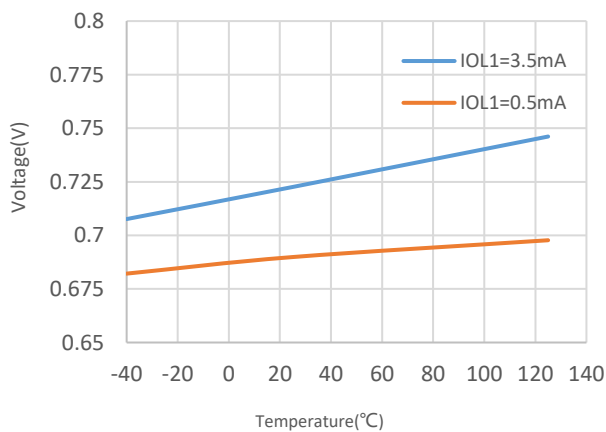


Figure 5. Side 1: Output Low Voltage vs Free-Air Temperature

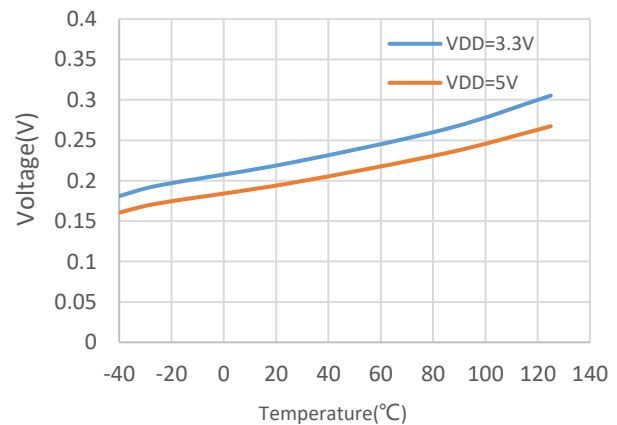


Figure 6. Side 2: Output Low Voltage vs Free-Air Temperature, Sink 35mA

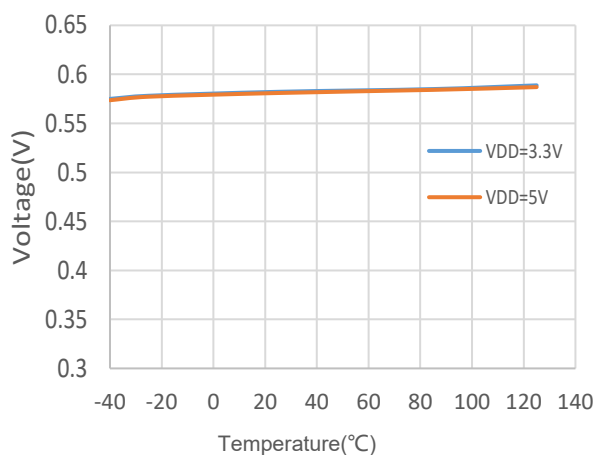


Figure 7. Side 1: Input Threshold High vs Free-Air Temperature

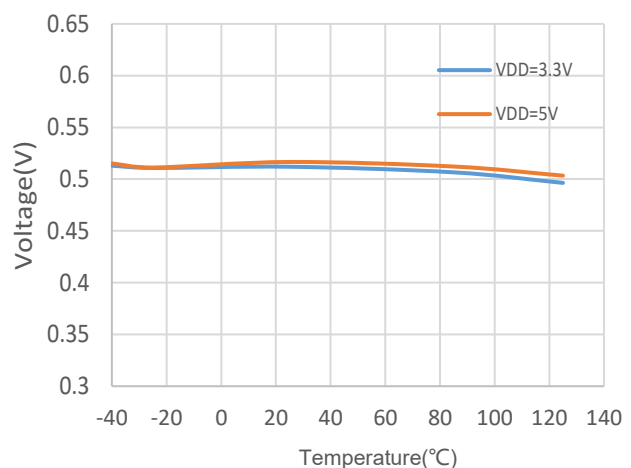


Figure 8. Side 1: Input Threshold Low vs Free-Air Temperature

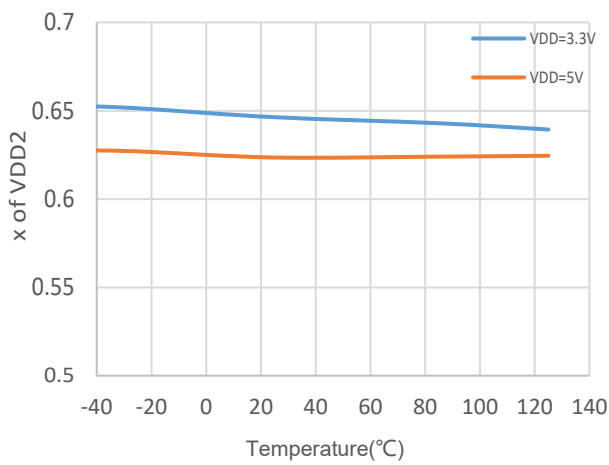


Figure 9. Side 2: Input Threshold High vs Free-Air Temperature

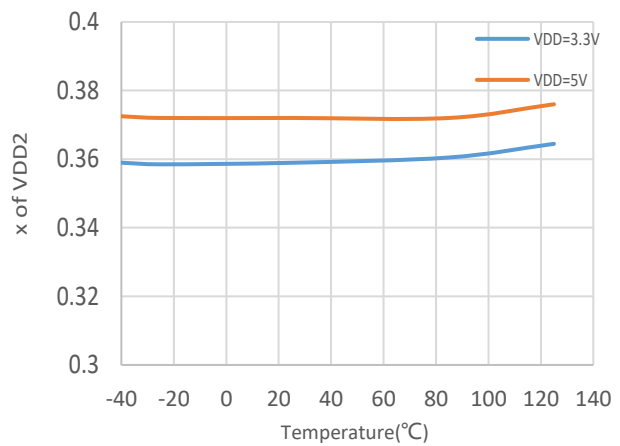


Figure 10. Side 2: Input Threshold Low vs Free-Air Temperature

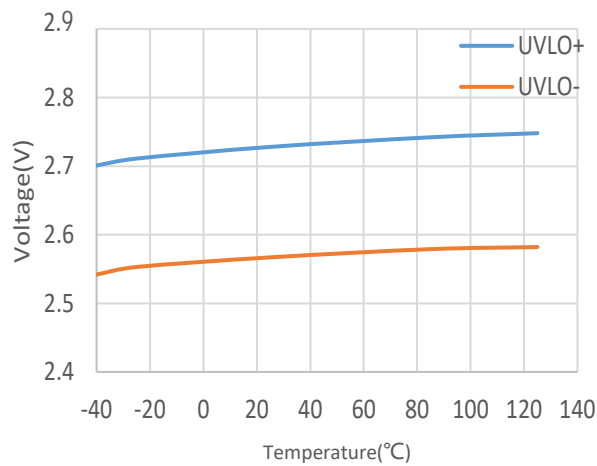


Figure 11 UVLO vs Free-Air Temperature

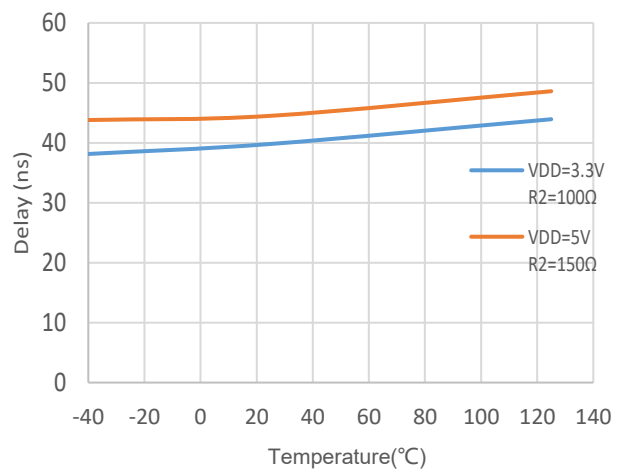


Figure 12. t_{PLH1-2} Propagation Delay vs Free-Air Temperature

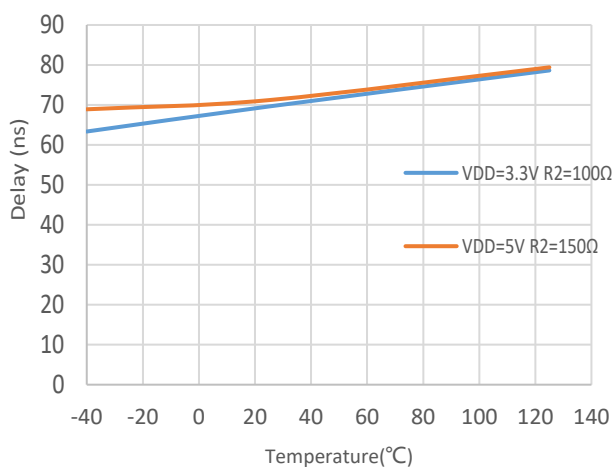


Figure 13. t_{PHL1-2} Propagation Delay vs Free-Air Temperature

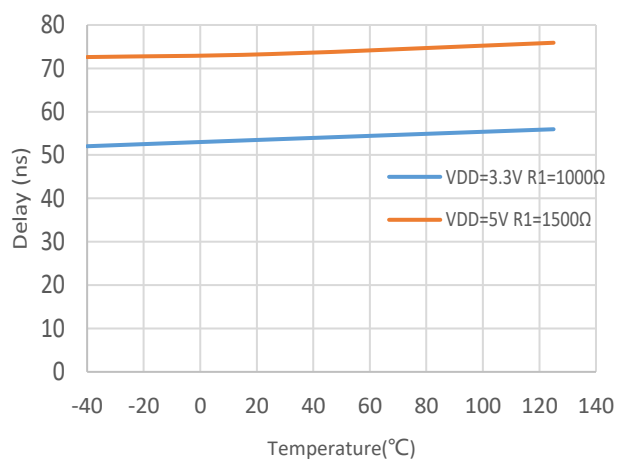


Figure 14. t_{PLH2-1} Propagation Delay vs Free-Air Temperature

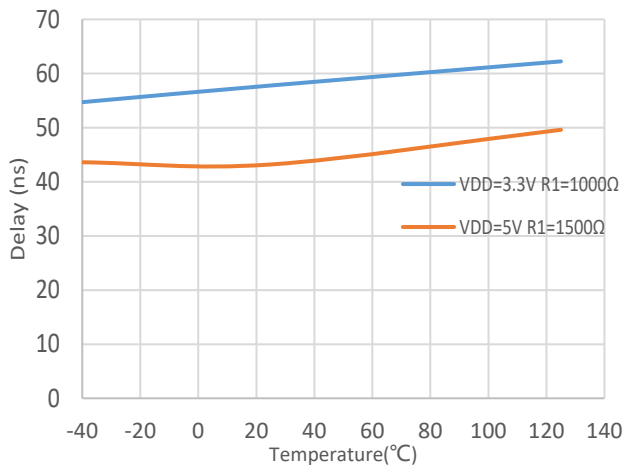


Figure 15. t_{PHL2-1} Propagation Delay vs Free-Air Temperature

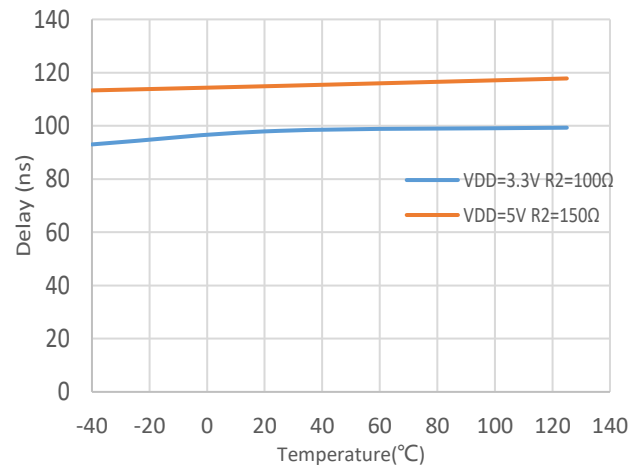


Figure 16. t_{LOOP1} vs Free-Air Temperature

Timing Test Information

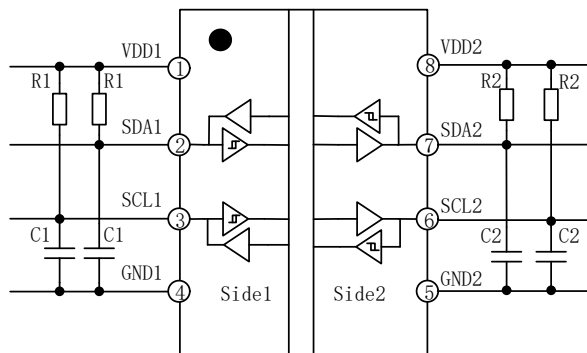


Figure 17. Test Diagram

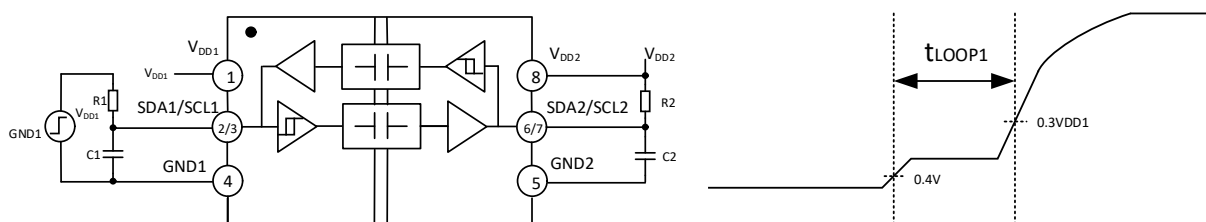


Figure 18. t_{Loop1} Setup and Timing Diagram

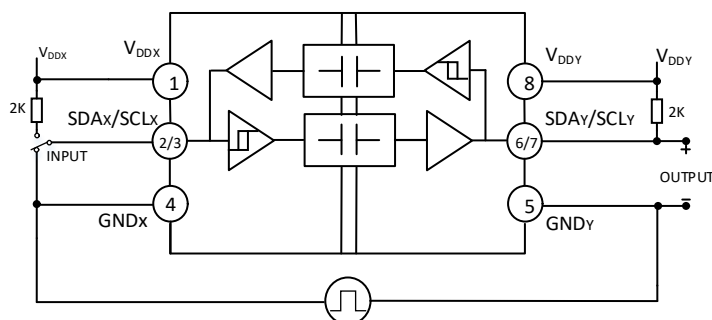


Figure 19. Common-Mode Transient Immunity Test Circuit



Applications Information

Overview

The inter-integrated circuit (I²C) bus is a single-ended, two wire bus for efficient inter-IC communication and is used in a wide range of applications. The I²C bus is used for communication between multiple masters or a single master and slaves. The master device controls the serial clock line (SCL), and data is bidirectional transferred on the serial data line (SDA) between master and slaves. The I²C bus can theoretically add up to 112 communication nodes, however, the number of nodes will increase the load capacitance on the bus, thereby limiting the communication distances and communication speeds. In applications, tradeoffs are often made between communication speeds, bus length, and number of nodes based on actual conditions.

The I²C bus supports data transmission in four speeds: standard mode (up to 100Kbps), fast mode (up to 400Kbps), fast mode plus (up to 1Mbps), and high-speed mode (up to 3.4Mbps). The ISO1540DR device support all the above four communication modes.

Functional Description

The ISO1540DR device is low-power bidirectional isolators compatible with the I²C interface.

This device have logic input and output buffers that are separated by using a silicon dioxide (SiO₂) barrier. This device block high voltages and prevent noise currents from entering the control side ground, avoiding circuit interference, and damaging sensitive components.

Each channel output of the ISO1540DR device is made open-drain to comply with the open-drain technology of I²C. Serial data line (SDA) and serial clock line (SCL) need to add pull-up resistors to ensure normal operation of the system. It is recommended that side 1 of the I²C isolator be connected to the processor and sides 2 to the bus when there are multiple nodes on the I²C bus as side 2 support up to 400pF capacitance load.

The ISO1540DR device feature two bidirectional channels that have open-drain outputs, As shown in Figure 20. As a logic low on one side causes the corresponding pin on the other side to be pulled low, to avoid data-latching within the device, The output logic low (V_{OL1}) voltages of SDA₁ and SCL₁ are at least 60mV higher than the input threshold high (V_{IHT1}) of SDA₁ and SCL₁, As shown in Figure 21.

Because the Side 2 logic levels/thresholds are standard I²C values, multiple ISO1540DR devices connected to a bus by their Side 2 pins can communicate with each other and with other I²C compatible devices. However, because the Side 1 pin has a modified output level/ input threshold, this side of the ISO1540DR can communicate only with devices that conform to the I²C standard.

The output low voltages of ISO1540DR device is guaranteed for sink currents of up to 35mA for side 2, and 3.5mA for side 1.

To enhance system reliability, it is recommended to connect the node with larger load capacitance and longer wires on side 2 for point-to-point communication.

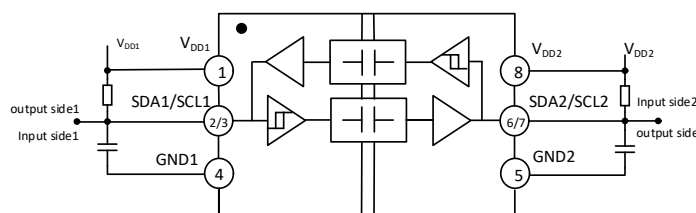


Figure 20. system operation diagram

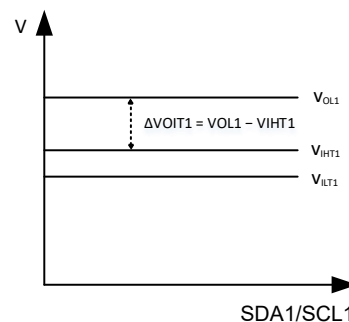


Figure 21. side 1 voltage Diagram



Typical Application Diagram

Figure 22 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2. Bypass capacitors with values from 0.1 μ F to 10 μ F are required between VDD1 and GND1 and between VDD2 and GND2. To enhance the robustness of a design, the user may connect a resistor (50-200 Ω) in series between R2 and C1 and between R3 and C2 if the system is excessively noisy.

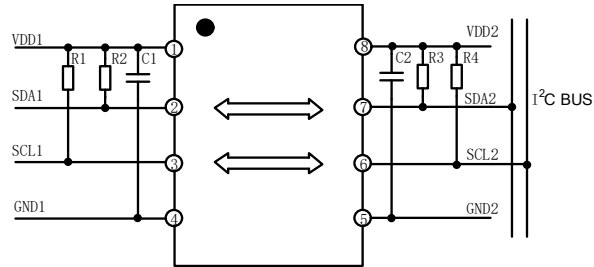
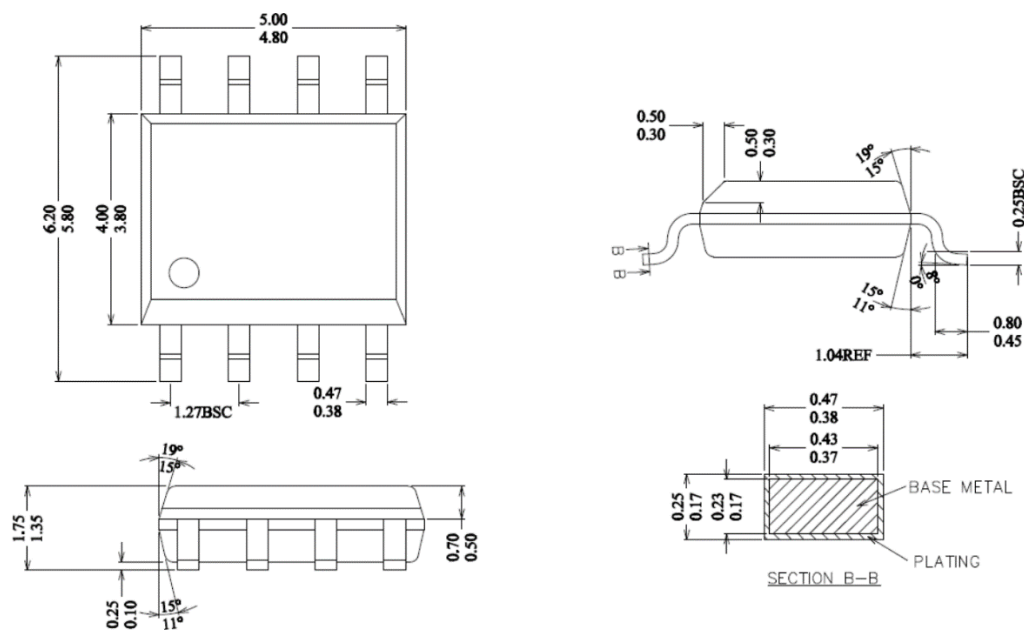


Figure 22. Typical Isolated I²C Interface Using the ISO1540DR



Outline Dimensions



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure 23. 8-Lead SOP Outline Package—dimension unit(mm)

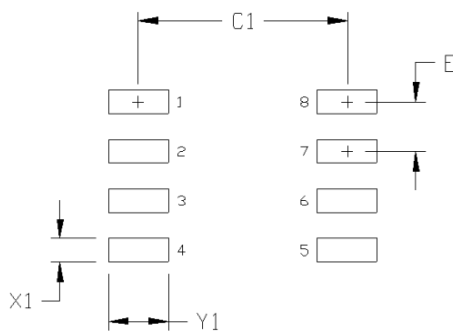


Figure 24.8-Lead SOP Land Pattern

Table 12.8-Lead SOP Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

Note:

- 1.This land pattern design is based on IPC -7351.
- 2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.



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