## Descriptions

The NVT4557HKX device is built for interfacing a SIM card with a single low-voltage 1.0V to 1.8 V host side interface. The NVT4557HKX contains three 1.62 V to 3.6 V level translators to convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller. The NVT4557HKX is compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements.

## Order Information

| Package | | Part Number | Top-Side Marking |
|---|---|---|---|
| QFN1418(XQFN-10(1.4x1.8)) | Tape and Reel | NVT4557HKX | ##### |

## Features

- Supports clock speed up to 10 MHz clock
- Compliant with all ETSI, IMT-2000 and ISO-7816 SIM/Smart card interface requirements
- Support SIM card supply voltages with range of 1.62 V to 3.6 V
- Host microcontroller operating voltage range: 1.08 V to 1.98 V
- Automatic level translation of I/O, RSTn and CLKn between SIM card and host side interface with capacitance isolation
- Incorporates shutdown feature for the SIM card signals according to ISO-7816-3
- Automatic enable and disable through VCCB (Enable pin on A4557 Q 10 pin package only)
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on VCCB or any of the card side pins. External ESD diodes are not required.
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Available in 10-pin QFN10 package with 0.4mm pitch

## Applications

- Mobile, Smart phones and Wireless modems
- SIM card terminals

## Functions and Pin Configuration

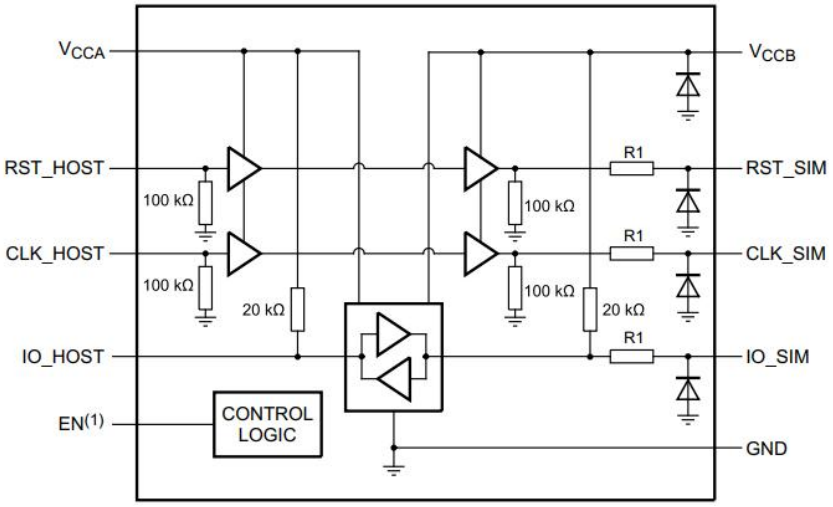
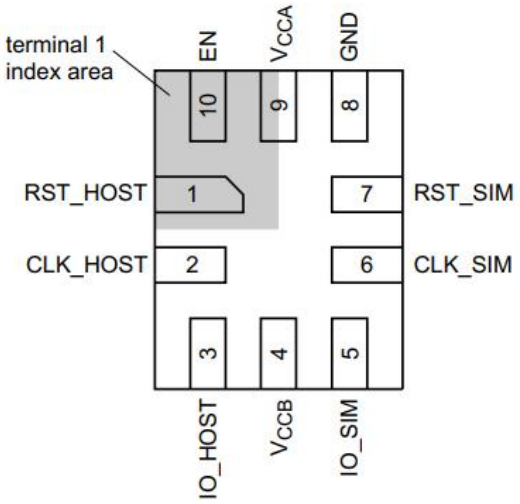



**Fig.1 Functional Diagram**



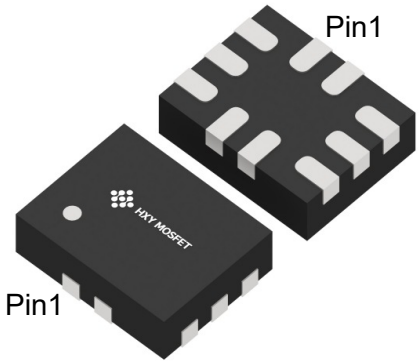




**Fig.2 QFN1418(XQFN-10(1.4x1.8))**

## Pin Descriptions

| Name | Pin for CSP | Pin for QFN | Type | Description |
|---|---|---|---|---|
| RST_HOST | A1 | 1 | I | Reset input from host controller |
| VCCA | A2 | 9 | Supply | Supply voltage for the host controller side input/output pins (CLK_HOST, RST_HOST, IO_HOST). This pin should be bypassed with a 0.1 μF ceramic capacitor close to the pin. |
| RST_SIM | A3 | 7 | O | Reset output pin for the SIM card |
| CLK_HOST | B1 | 2 | I | Clock input from host controller |
| GND | B2 | 8 | GND | Ground for the SIM card and host controller. Proper grounding and bypassing are required to meet ESD specifications |
| CLK_SIM | B3 | 6 | O | Clock output pin for the SIM card |
| IO_HOST | C1 | 3 | I/O | Host controller bidirectional data input/output. The host output must be on an open-drain driver |
| VCCB | C2 | 4 | Supply | SIM card supply voltage. When VCCB is below the VCCBdisable, the device is disabled. This pin should be bypassed with a 0.1 μF ceramic capacitor close to the pin |
| IO_SIM | C3 | 5 | I/O | SIM card bidirectional data input/output. The SIM card output must be on an open-drain driver |
| EN | --- | 10 | I | Host controller driven enable pin. This pin should be HIGH (VCCA) for normal operation, and LOW to help avoid race conditions specifically during the shutdown sequence. (Only on 10 pin version - for 9 pin version EN is pulled to VCCA.) |

**Table-1 Pin Descriptions**

### Shutdown Sequence of NVT4557HKX (10-pin version only)

The ISO 7816-3 specification specifies the shutdown sequence for the SIM card signals to ensure that the card is properly disabled for power savings. Also during hot swap, the orderly shutdown of these signals helps to avoid any improper write and corruption of data. When the enable, EN, is asserted LOW, the shutdown sequence is initiated by powering down the RST_SIM channel. Once the RST_SIM channel is powered down, CLK_SIM and IO_SIM are powered down sequentially one-by-one. An internal pull-down resistor on the SIM pins is used to pull these channels LOW. The shutdown sequence is completed in a few microseconds. It is important that EN is pulled LOW before VCCA and VCCB supplies go LOW to ensure that the shutdown sequence is properly initiated.

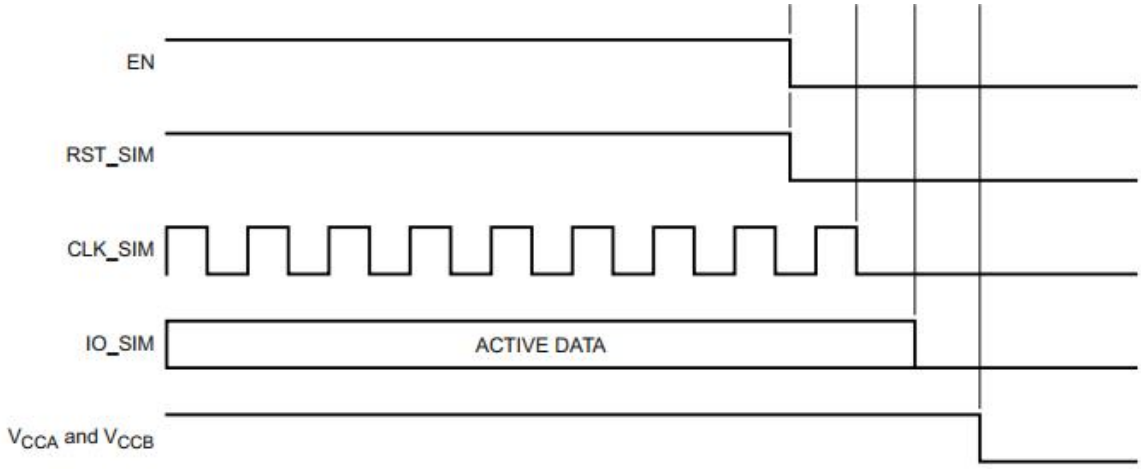



**Fig.3 Shutdown sequence for RST_SIM, CLK_SIM, IO_SIM and VCCA/VCCB**

### Level Translator Stage

The architecture of the device I/O channel is shown below. The device does not require an extra input signal to control the direction of data flow from host to SIM or from SIM to host. As a change of driving direction is just possible when both sides are in HIGH state, the control logic is recognizing the first falling edge granting it control about the other signal side. During a rising edge signal, the non-driving output is driven by a one shot circuit to accelerate the rising edge. In case of a communication error or some other unforeseen incident that would drive both connected sides to be drivers at the same time, the internal logic automatically prevents stuck-at situation, so both I/Os will return to HIGH level once released from being driven LOW. The channels RST and CLK just contain single direction drivers without the holding mechanism of the I/O channel, as these are just driven from the host to the card side.

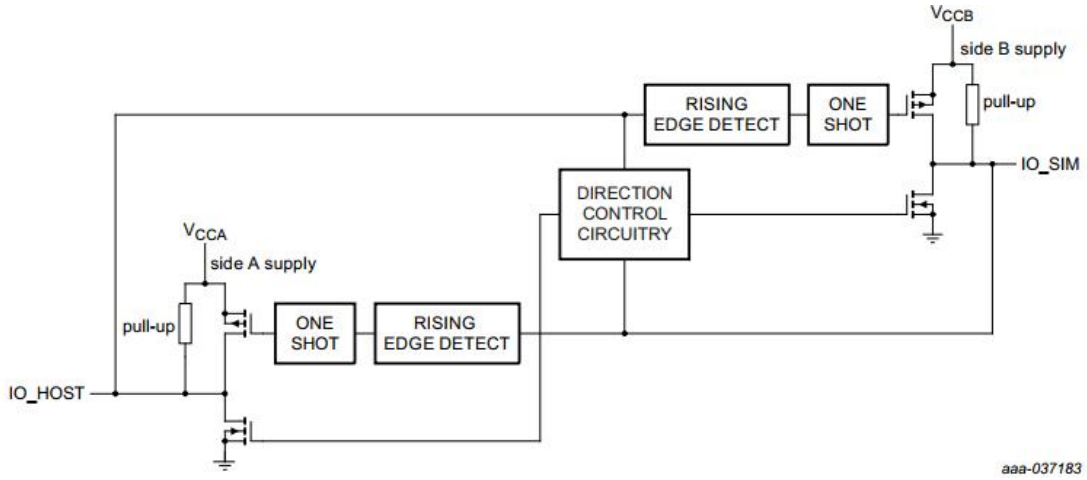



**Fig.4 Automatic direction control level translator for HIGH-level direction change interfaces**

**Electrical Characteristics** (Ta=25°C, $V_{VCCA}$ =1.0V~1.8V,$V_{VCCB}$ =1.62V~3.6V, unless otherwise specified)

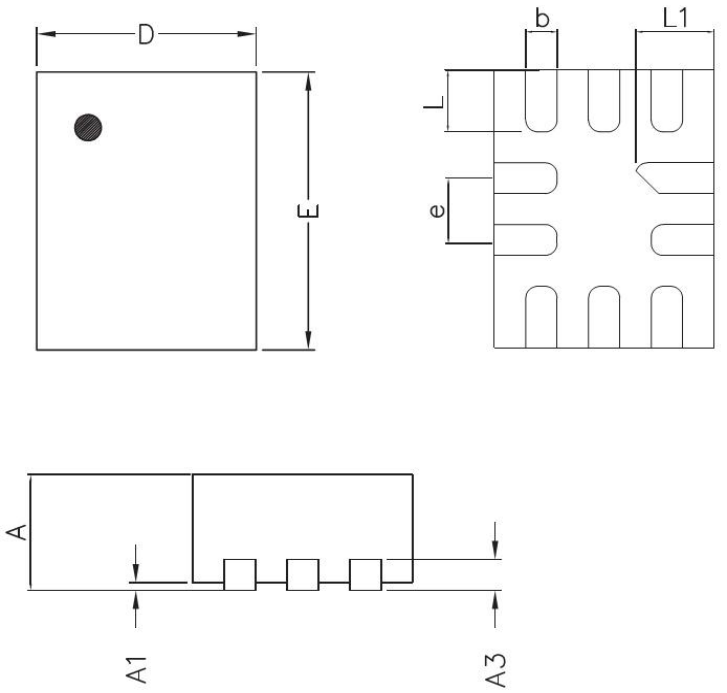
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supplies | | | | | | |
| VCCA | Host Side Supply | | 1.0 | | 1.98 | V |
| VCCB | SIM Side Supply | | 1.6 | | 3.6 | V |
| $V_{VCCA\_UVLO}$ | VCCA Under Voltage Lockout | Rising, 100mV hysteresis | 0.6 | 0.7 | 0.8 | V |
| $V_{VCCB\_UVLO}$ | VCCB Under Voltage Lockout | Rising. 100mV hysteresis | 1.3 | 1.4 | 1.5 | V |
| $I_{SD\_VCCA}$ | Shutdown Current EN=0V | VCCA=1.2V | | 0.5 | 1 | uA |
| $I_{SD\_VCCB}$ | | VCCB=1.8V | | 0.5 | 1 | uA |
| $I_{Q\_VCCA}$ | Quiescent Current EN=VCCA | VCCA=1.2V, CLK_HOST=0V | | 0.5 | 1 | uA |
| $I_{Q\_VCCB}$ | | VCCB=1.8V, CLK_HOST=0V | | 0.5 | 1 | uA |
| $I_{ACT\_VCCA}$ | Active Current EN=VCCA | VCCA=1.2V, CLK_HOST=1MHz CL= 30pF | | 5 | 10 | uA |
| $I_{ACT\_VCCB}$ | | VCCB=1.8V, CLK_HOST=1MHz CL= 30pF | | 250 | 300 | uA |
| Logic I/O pin (EN) | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | EN pin | 0.7*VCCA | | | V |
| $V_{IL}$ | Low-Level Input Voltage | EN pin | | | 0.3*VCCA | V |
| Level Translator (Host Side) | | | | | | |
| $V_{IH}$ | High Level input voltage | IO_HOST, RST_HOST, CLK_HOST | 0.7*VCCA | | | V |
| $V_{IL}$ | Low Level input Voltage | IO_HOST, RST_HOST, CLK_HOST | | | 0.3*VCCA | V |
| $V_{OH}$ | High Level output voltage | IO_HOST, IOH_IO=20uA | 0.8*VCCA | | | V |
| $V_{OL}$ | Low Level output voltage | IO_HOST, IOL_IO=20uA | | | 0.2*VCCA | V |
| $R_{PUA}$ | Pull up resistance | IO_HOST connected to VCCA | 6 | 8 | 10 | kΩ |
| Level Translator (SIM Card Side) | | | | | | |
| $V_{IH}$ | High Level input voltage | IO_SIM | 0.7*VCCB | | | V |
| $V_{IL}$ | Low Level input Voltage | IO_SIM | | | 0.3*VCCB | V |
| $V_{OH}$ | High Level output voitage | CLK_SIM, RST_SIM, IOH=20uA | 0.8*VCCB | | | V |
| | | IO_SIM, IOH=20uA | 0.8*VCCB | | | V |
| $V_{OL}$ | Low Level output voltage | CLK_SIM, RST_SIM, IOL =-1mA | | | 0.125*VCCB | V |
| | | IO_SIM, IOL =-1mA | | | 0.125*VCCB | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| $R_{PUB}$ | Pull up resistance | IO_SIM connected to VCCB | 12 | 20 | 30 | kΩ |
| Rs | Series resistance | IO_SIM, RST_SIM, CLK_SIM | 40 | 55 | 100 | Ω |
| $R_{PD}$ | Pull down resistance | IO_SIM, RST_SIM, CLK_SIM when EN is driven low | | 4 | | kΩ |
| Dynamic Characteristics (CL=30pE in Host side, CL=30Pf in SIM side, VCCA=1.8V, VCCB=3.0V) | | | | | | |
| $t_{PD}$ | Propagation delay | From Host side to SIM side | | 10 | 20 | ns |
| $t_{PD}$ | Propagation delay | From SIM side to HOST side | | 10 | 20 | ns |
| $t_{r\_B}$ | RST_SIM Rising time | From 10% to 90% of VCCB=3.0V | | 8 | 15 | ns |
| | CLK_SIM Rising time | From 10% to 90% of VCCB=3.0V | | 8 | 15 | ns |
| | IO_SIM Rising time | From 10% to 90% of VCCB=3.0V | | 8 | 15 | ns |
| $t_{r\_B}$ | RST SIM falling time | From 90 %to 10% of VCCB=3.0V | | 8 | 15 | ns |
| | CLK_SIM falling time | From 90 %to 10% of VCCB=3.0V | | 8 | 15 | ns |
| | IO_SIM falling time | From 90 %to 10% of VCCB=3.0V | | 8 | 15 | ns |
| $t_{r\_A}$ | IO_HOST rising time | From 10% to 90% of VCCA=1.8V | | 8 | 15 | ns |
| $t_{r\_A}$ | IO_HOST falling time | From 90 %to 10% of VCCA=1.8V | | 8 | 15 | ns |
| $t_{EN}$ | Enable timing | From EN High to RST_High | | | 100 | ns |
| $t_{RST\_DIS}$ | RST_SIM Disable time | From EN Low to RST_SIM low | | 200 | | ns |
| $t_{CLK\_DIS}$ | CLK_SIM Disable time | From EN low to CLK_SIM low | | 15 | | us |
| $t_{IO\_DIS}$ | IO_SIM Disable time | From EN low to IO_SIM low | | | | us |
| $f_{CLK}$ | CLK_HOST frequency | | | | 10 | MHZ |

**Table-2 Electrical Characteristics**

## Package Outline Dimensions

**QFN1418(XQFN-10(1.4x1.8))**




| Symbol | Dimension in Millimeters | |
|---|---|---|
| | Min. | Max. |
| A | 0.450 | 0.550 |
| A1 | 0.000 | 0.050 |
| A3 | 0.152 Ref. | |
| D | 1.350 | 1.450 |
| E | 1.750 | 1.850 |
| b | 0.150 | 0.250 |
| e | 0.400 Typ. | |
| L | 0.350 | 0.450 |
| L1 | 0.450 | 0.550 |

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