Descriptions

FSA644UCX is a high performance four-data lane MIPI, D-PHY or three-data lane MIPI, C-PHY switch. This single-pole,double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources.

The FSA644UCX has wide bandwidth and maintains good signal integrity,
which makes it ideal is designed for the MIPI specification and allows connection to a CSI or DS Imodule.

36 Ball Wafer Level Chip Scale Package (WLCSP) 2.4mm x 2.4mm with Pb-free and Halogen-free, makes it ideal for mobile device.

Order Information

Package		Part Number	Top-Side Marking
CSP-36(WLCSP-36)	Tape and Reel	FSA644UCX	A644

Features

- Pin-to-Pin FSA644, CSP-36(WLCSP-36)
- Signal Types: MIPI D-PHY and C-PHY
- Wide VCC Supply Range: 1.65v~5.5v
- Low Quiescent Current: 28uA Typical when VCC=1.8V
- Insertion loss: -1dB@1GHz, -2dB@1.5GHz, -3dB@2.5GHz
- Channel-to-Channel Cross-talk: -30dB Typical
- Power-off Truly Isolated and Off-Isolation: -25dB Typical

Applications

- Laptop, Multi-Camera and Displays, 4G/5G Smart Phone, Mobile and AI Device

Functional Diagram

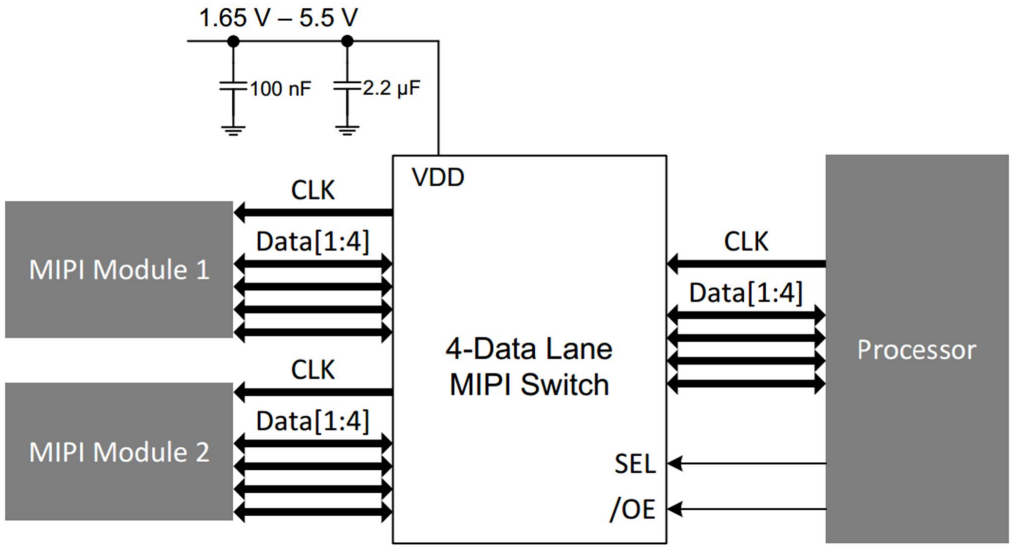


Fig.1 Functional Diagram

Pin Configuration

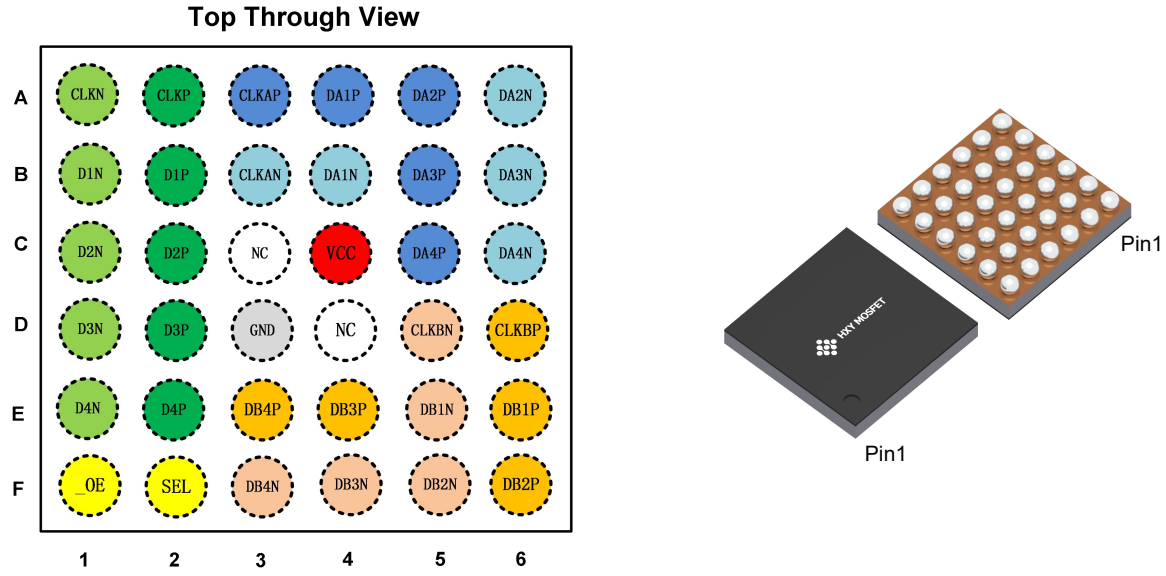


Fig.2 Top-Through View and Top-Side View

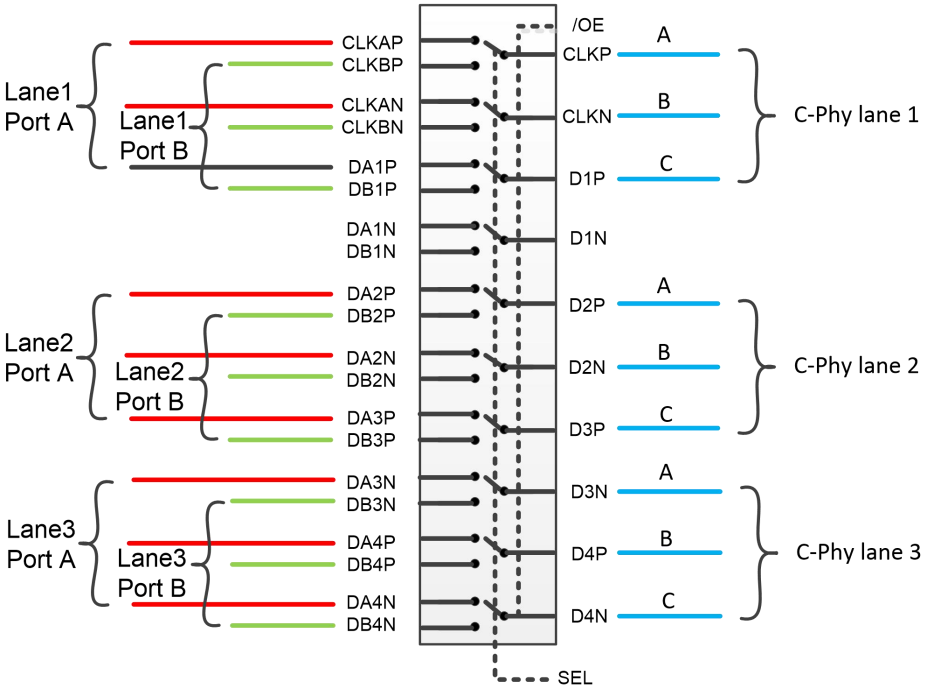


Fig.3 Recommended C-PHY Configuration

Pin Descriptions

Pin #	Name	Type	Description
A1	**CLKN**	I/O	Common Side Clock Path Negative
A2	**CLKP**	I/O	Common Side Clock Path Positive
A3	**CLKAP**	I/O	A Side Clock Path Positive
A4	**DA1P**	I/O	A Side Data Path 1 Positive
A5	**DA2P**	I/O	A Side Data Path 2 Positive
A6	**DA2N**	I/O	A Side Data Path 2 Negative
B1	**D1N**	I/O	Common Side Data Path 1 Negative
B2	**D1P**	I/O	Common Side Data Path 1 Positive
B3	**CLKAN**	I/O	A Side Clock Path Negative
B4	**DA1N**	I/O	A Side Data Path 1 Negative
B5	**DA3P**	I/O	A Side Data Path 3 Positive
B6	**DA3N**	I/O	A Side Data Path 3 Negative
C1	**D2N**	I/O	Common Side Data Path 2 Negative
C2	**D2P**	I/O	Common Side Data Path 2 Positive
C3	**NC**	O	Not Connected
C4	**VCC**	PWR	1.5~5V Positive Supply
C5	**DA4P**	I/O	A Side Data Path 4 Positive
C6	**DA4N**	I/O	A Side Data Path 4 Negative
D1	**D3N**	I/O	Common Side Data Path 3 Negative
D2	**D3P**	I/O	Common Side Data Path 3 Positive
D3	**GND**	GND	Primary Ground Connection. Must be Connected to System Ground
D4	**NC**	O	Not Connected
D5	**CLKBN**	I/O	B Side Clock Path Negative
D6	**CLKBP**	I/O	B Side Clock Path Positive
E1	**D4N**	I/O	Common Side Data Path 4 Negative
E2	**D4P**	I/O	Common Side Data Path 4 Positive
E3	**DB4P**	I/O	B Side Data Path 4 Positive
E4	**DB3P**	I/O	B Side Data Path 3 Positive
E5	**DB1N**	I/O	B Side Data Path 1 Negative
E6	**DB1P**	I/O	B Side Data Path 1 Positive
F1	**_OE**	I	Chip Enable, Low Active
F2	**SEL**	I	Channel Selection. When Low, A side selected; When High, B side selected
F3	**DB4N**	I/O	B Side Data Path 4 Negative
F4	**DB3N**	I/O	B Side Data Path 3 Negative
F5	**DA2N**	I/O	A Side Data Path 2 Negative
F6	**DA2P**	I/O	A Side Data Path 2 Positive

Table-1 Pin Descriptions

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1)

		Range	Unit
Power Supply Voltage	VCC	-0.5 ~ 6.0	V
Control Pins	_OE, SEL	-0.5 ~ VCC	V
DC Switch I/O Voltage	V_{SW}	-0.3 ~ VCC	V
DC I/O Current	I_{IK}	-50 ~ 50	mA
Storage Temperature Range	T_{STG}	-55 ~ 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001-2012	VCC	±2	kV
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV
ESD MM, JESD22-A115	VCC	±200	V
	_OE, SEL	±2	kV
	Other I/O Pins	±2	kV

Table-2 Absolute Maximum Ratings

(1) Stresses beyond those listed in Table-2 *Absolute Maximum Ratings* may cause permanent damage to the device. They are stress ratings only, which do not imply functional operation of the device at these or any other conditions. Beyond those indicated under *Recommended Operating Conditions*, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommend Operating Conditions

		Range	Unit
Power Supply Voltage	VCC	1.65 ~ 5.5	V
Control Pins	_OE, SEL	0 ~ VCC	V
Signal Pins	HS Mode	0 ~ 0.3	V
	LP Mode	0 ~ 1.3	V
Operating Temperature	T_A	-40 ~ 85	°C

Table-3 Recommend Operating Conditions

(1) If _OE is left undriven, it will be pulled up to VCC by internal resistor; If SEL is left undriven, it will be pulled down to Ground by internal resistor.

Electrical Characteristics (Ta=25°C, VCC=1.8V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
VCC Quiescent Current	I_Q	SEL=0 or VCC, _OE=0		28		uA
Power-down Current	I_{PD}	SEL=0 or VCC, _OE=VCC			1	uA
DC Characteristics						
Input logic high	V_{IH}	VCC=1.8~4.5V	1.6			V
Input logic low	V_{IL}	VCC=1.8~4.5V			0.4	V
_OE Internal pull-up resistor	R_{UP}			2		MΩ
SEL Internal pull-down resistor	R_{DN}			2		MΩ
On-Resistance for LP MIPI	R_{ON_LP}	V_{IS}= 1.2V I_{ON}=8mA		7.5	9	Ω
On-Resistance for HS MIPI	R_{ON_HS}	V_{IS}= 0.2V I_{ON}=8mA		6.7	8	Ω
R_{ON} Flatness for LP MIPI	R_{FLAT_LP}	V_{IS}= 0 to 1.2V I_{ON}=8mA		0.8	1	Ω
R_{ON} Flatness for HS MIPI	R_{FLAT_LP}	V_{IS}= 0 to 0.2V I_{ON}=8mA		0.2	0.3	Ω
R_{ON} Matching Between Channels	R_{MATCH}	V_{IS}= 0 to 1.2V I_{ON}=8mA		0.1		Ω
Switch Off Leakage Current	I_{OFF}	_OE=VCC Dn, Dp =VCC DAn, DBn, DAp, DBp=0 CLKn, CLKp=0 CLKAn, CLKBn, CLKAp, CLKBp=VCC	-0.5		0.5	uA
AC Characteristics						
Enable Time _OE to Output	t_{EN}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		80	150	uS
Disable Time _OE to Output	t_{DIS}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		40	250	nS
Turn-On Time SEL to Output	t_{ON}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		400	1200	nS
Turn-Off Time SEL to Output	t_{OFF}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		130	800	nS
Break-Before-Make Time	t_{BBM}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		250	500	nS
Propagation Delay	t_{PD}	R_L=50Ω C_L=0pF V_{IS}= 0.6V		0.25		nS
Off Isolation	Off	R_L = 50Ω f =1.2GHz V_{IS}= 0.2V_{PP}		-33		dB
Crosstalk (Channel-to-Channel)	X_{TALK}	R_L = 50Ω f =1.2GHz V_{IS}= 0.2V_{PP}		-43		dB
-3dB Bandwidth (Insertion Loss)	BW_{-3dB}	R_L=50Ω C_L=0pF Signal 0dBm	2.5	3.5		GHz
Capacitance						
Switch On Capacitance	C_{ON}	V_{Bias} = 0.2V, f = 1MHz		1.5		pF
Switch Off Capacitance	C_{OFF}	V_{Bias} = 0.2V, f = 1MHz		1.0		pF

Table-4 Electrical Characteristics

Note:

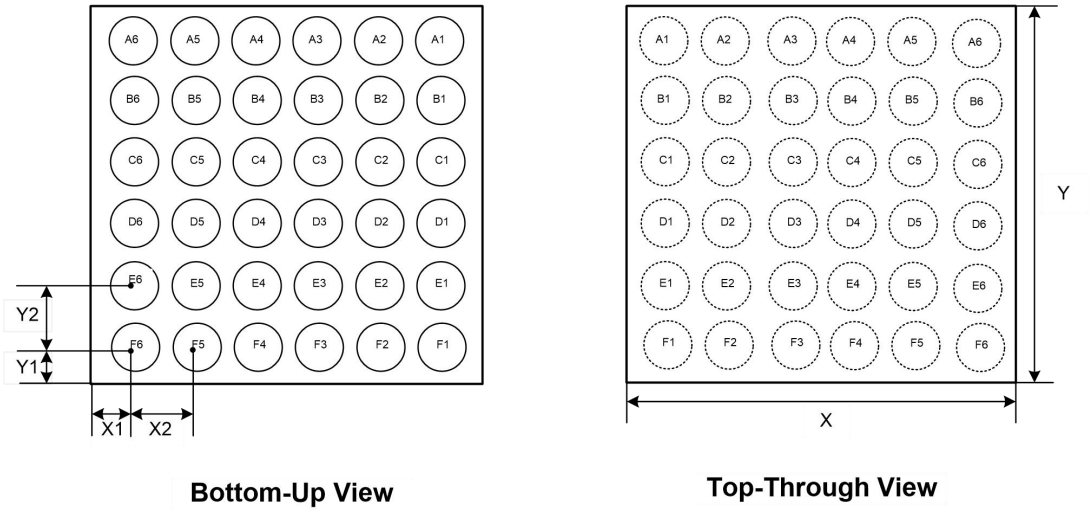
(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

Package Outline Dimensions

CSP-36(WLCSP-36)



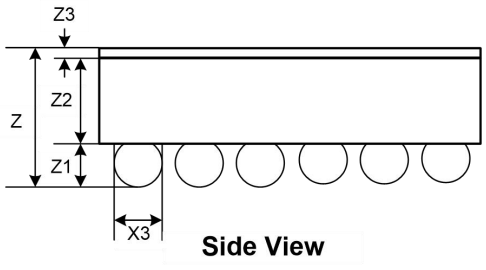
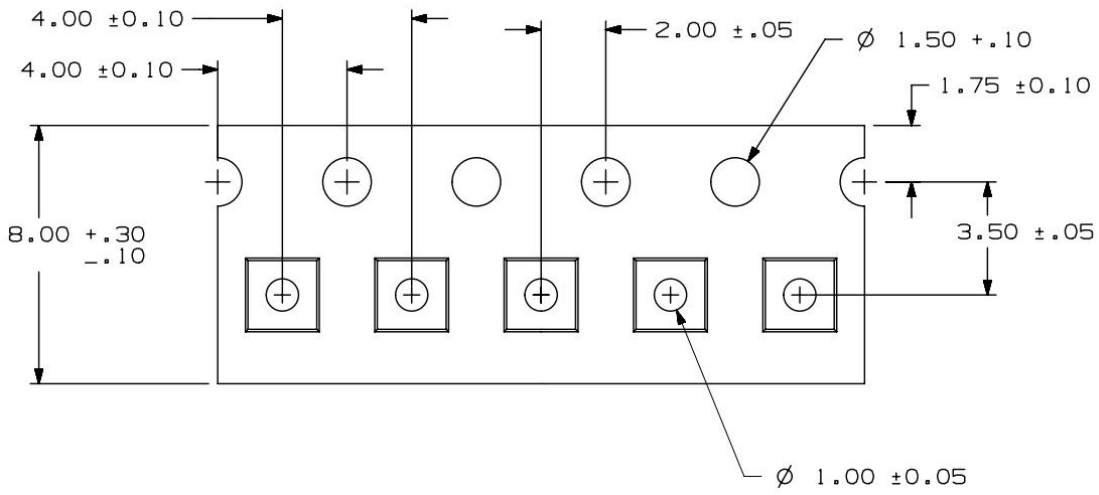


Fig.3 Package Outline Dimensions

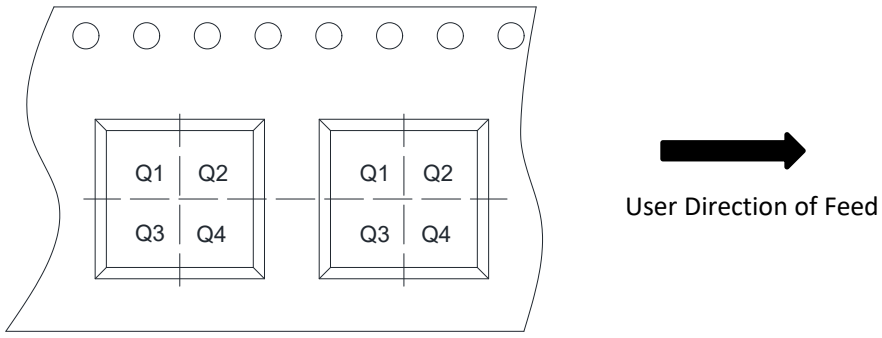
Symbol	Dimensions In Millimeter		
	Min.	Typ.	Max.
X	2.37	2.40	2.43
Y	2.37	2.40	2.43
X1		0.16	
X2		0.40	
X3	0.175	0.205	0.235
Y1		0.16	
Y2		0.40	
Z	0.550	0.600	0.650
Z1	0.145	0.170	0.195
Z2	0.340	0.365	0.390
Z3	0.395	0.040	0.045

Table-5 Package Outline Dimensions

Tape and Reel Information



Quadrant Assignments for PIN 1 Orientation In Tape



Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

Fig.4 Tape and Reel Information

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