Descriptions

The TS5USBC412YFFR is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C™ systems. The device is configured as a dual 2:1 or 1:2 switch. It is optimized for use with the USB 2.0 DP/DM lines in a USB Type-C™ system.

The TS5USBC412YFFR integrated over-voltage protection on the D+/- pins can withstand up to DC 30V with automatic shutoff circuitry in order to protect system components behind the switch. GPIO controls of S1, S2 and _OE are 1.8V logic compatible. The TS5USBC412YFFR is available in 12 Ball Wafer Level Chip Scale Package (CSP) with 1.2x1.6x0.6mm with Pb-free and Halogen-free making it a perfect candidate for mobile and space constrained applications.

Order Information

Package		Part Number	Top-Side Marking
CSP-12(DSBGA-12)	Tape and Reel	TS5USBC412YFFR	UXYW

Features

- Pin-to-Pin MAX14743EWC, TS5USBC412, TS5USBC410, KTU1002AEVA, CSP-12(DSBGA-12)
- Supply Range 2.5 V to 5.5 V
- Differential 2:1 or 1:2 Switch/Multiplexer
- Up to DC 30V Overvoltage Protection (OVP) on D+/- Ports
- IEC 64000-4-5 Surge Protection w/o External TVS onto D+/- Ports: ±30V
- System Side Clamp Voltage Pulse Less than 9V, Duration Less than 200nS
- Powered Off Protection When VCC = 0 V
- Low RON of 10 Ω Typical
- Insertion loss: -1dB@200MHz, -2dB@650MHz, -3dB@1GHz
- C_{ON} of 4.8 pF
- 1.8-V Compatible Logic Inputs
- Standard Temperature Range of 0°C to 85°C

Applications

- Anywhere a USB Type-C™ or Micro-B Connector is Used
- Mobile Phones, Tablets and Notebooks

Functions and Pin Configuration

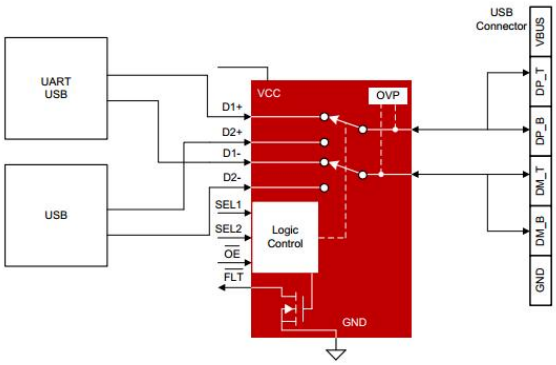


Fig.1 Functional Diagram

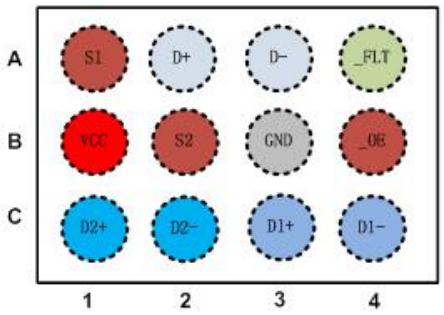


Fig.2 Top-Through View

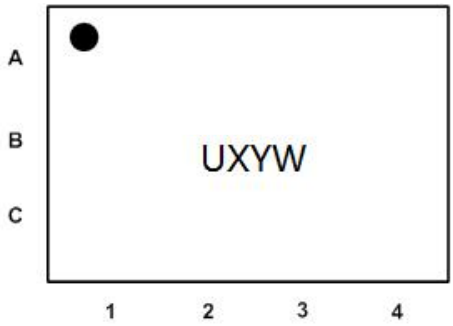
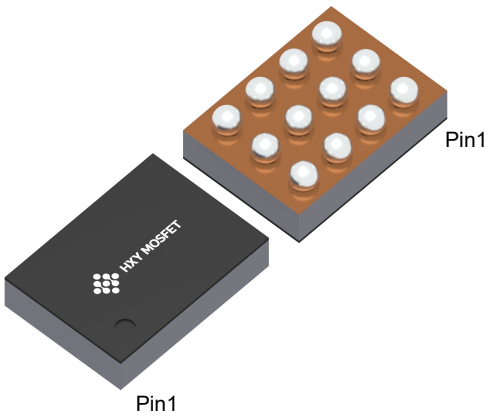


Fig.3 Top Side Marking View



CSP-12(DSBGA-12)

Pin Descriptions

Pin	Name	Type	Description
A1	S1	I	Switch Select 1 (Active High)
A2	D+	I/O	Data switch input (Differential +)
A3	D-	I/O	Data switch input (Differential -)
A4	_FLT	O	Fault indicator output (Active Low) open drain
B1	VCC	PWR	Power Supply
B2	S2	I	Switch Select 2 (Active High)
B3	GND	GND	Ground
B4	_OE	I	Output Enable (Active Low)
C1	D2+	I/O	Data switch output 2 (Differential +)
C2	D2-	I/O	Data switch output 2 (Differential -)
C3	D1+	I/O	Data switch output 1 (Differential +)
C4	D1-	I/O	Data switch output 1 (Differential -)

Table-1 Pin Descriptions

Electrical Characteristics (Ta=25°C, VCC=3.3V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
Supply Voltage Range	V_{CC}		2.5	3.3	5.5	V
Supply Current	I_{CC}	_OE =1 disconnection		0.6	2	uA
		_OE =0 connection		33		uA
S1/S2/_OE Digital Input Contol						
control input logic high	V_{IH}		1.6		5.5	V
control input logic low	V_{IL}		-0.1		0.5	V
Internal pull-down resistor	R_{PD}			2		MΩ
Switch On Resistance And Off Leakage						
On-Resistance	R_{ON}	V_{IS}= 0V~0.4V I_{OUT}=8mA		10	11	Ω
R_{ON} Flatness(1)	R_{FLAT}	V_{IS}= 0V~0.4V I_{OUT}=8mA		0.3	0.5	Ω
R_{ON} Matching Between Channels(2)	ΔR_{ON}	V_{IS}= 0V~0.4V I_{OUT}=8mA		0.1	0.2	Ω
OFF Leakage Current	I_{LEAK}	$V_{D+/-}$= 10V $V_{D1+/-}$= $V_{D2+/-}$ =0V		31	50	uA
Switch Dynamics						
On Capacitance	C_{ON}	$V_{D+/-}$ = 0.2V, f = 1MHz		4		pF
Off Capacitance	C_{OFF}	$V_{D+/-}$ = 0.2V, f = 1MHz		3		pF
Off Isolation	Off	f = 250MHz, R_T = 50Ω, C_L = 0pF		-38		dB
Crosstalk(3) (Channel-to-Channel)	X_{TALK}	f = 250MHz, R_T = 50Ω, C_L = 0pF		-41		dB
-3dB Bandwidth	BW	R_T=50Ω, C_L=0pF Signal Power 0dBm	0.9	1		GHz
Break-Before-Make	BBM	$V_{D1+/-}$ =$V_{D2+/-}$ =0.4V, R_L=50Ω		1.5		uS
Turn-on Time	t_{ON}	$V_{D+/-}$ = 0.4V, R_L=50Ω _OE switches from High to Low		20		uS
Turn-off Time	t_{OFF}	$V_{D+/-}$ = 0.4V, R_L=50Ω _OE switches from Low to High		1.2		uS
Propagation Delay	t_{PD}	$V_{D+/-}$ = 0.4V, R_L=50Ω		200		pS
Over Voltage Protection						
OVP Lockout Threshold	V_{OVP}	$V_{D+/-}$ Rising Edge	4.6	4.9	5.2	V
OVP Hysteresis	V_{HYS}	$V_{D+/-}$ Falling Edge		200		mV
Clamp Voltage on $D_{1+/-}$ and $D_{2+/-}$	V_{CLAMP}	10V shorts to $D_{+/-}$ with R_L=1KΩ @ $D_{1+/-}$ and $D_{2+/-}$		6.5	8	V
OVP Response Time	t_{FP}	10V shorts to $D_{+/-}$ with R_L=1KΩ @ $D_{1+/-}$ and $D_{2+/-}$		200	300	nS
OVP Recovery Time	t_{FPR}	$V_{D+/-}$ jumps from 6V to 1V step	30	45	60	uS

Table-2 Electrical Characteristics

Note:

(1) Flatness is defined as the difference between maximum and minimum value of ON-resistance at the specified analog signal voltage points.

(2) R_{ON} matching between channels is calculated by subtracting the channel with the lowest max Ron value from the channel with the highest max Ron value.

(3) Crosstalk is inversely proportional to source impedance

Typical Performance Curves (Ta=25°C, VCC=3.0V, CAP=0.1uF, unless otherwise noted)

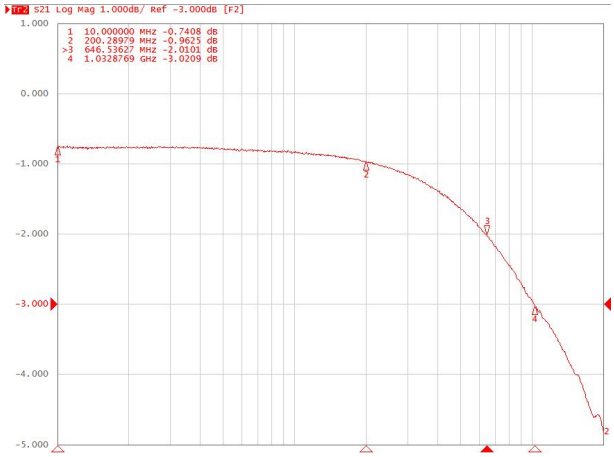


Fig.4 Switch Bandwidth or Insertion Loss

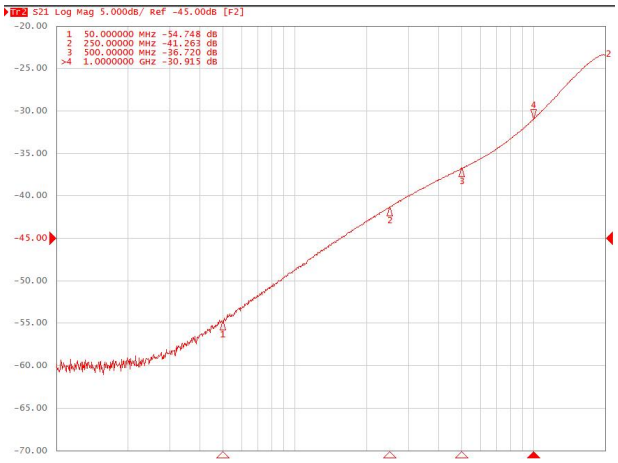


Fig.5 Switch Channel to Channel Cross-Talk

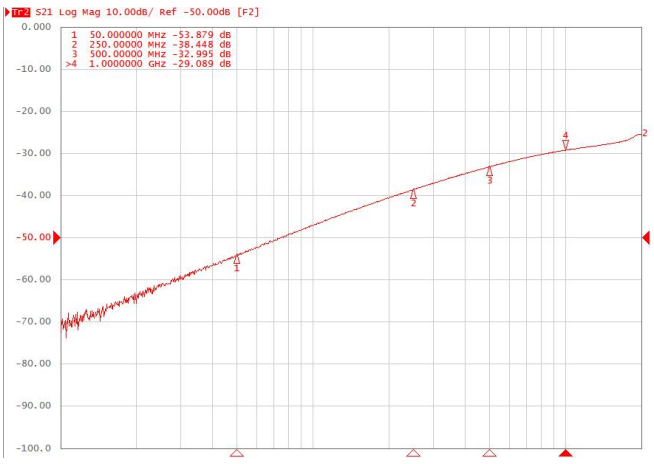


Fig.6 Switch Off Isolation

Package Outline Dimensions

CSP-12(DSBGA-12)

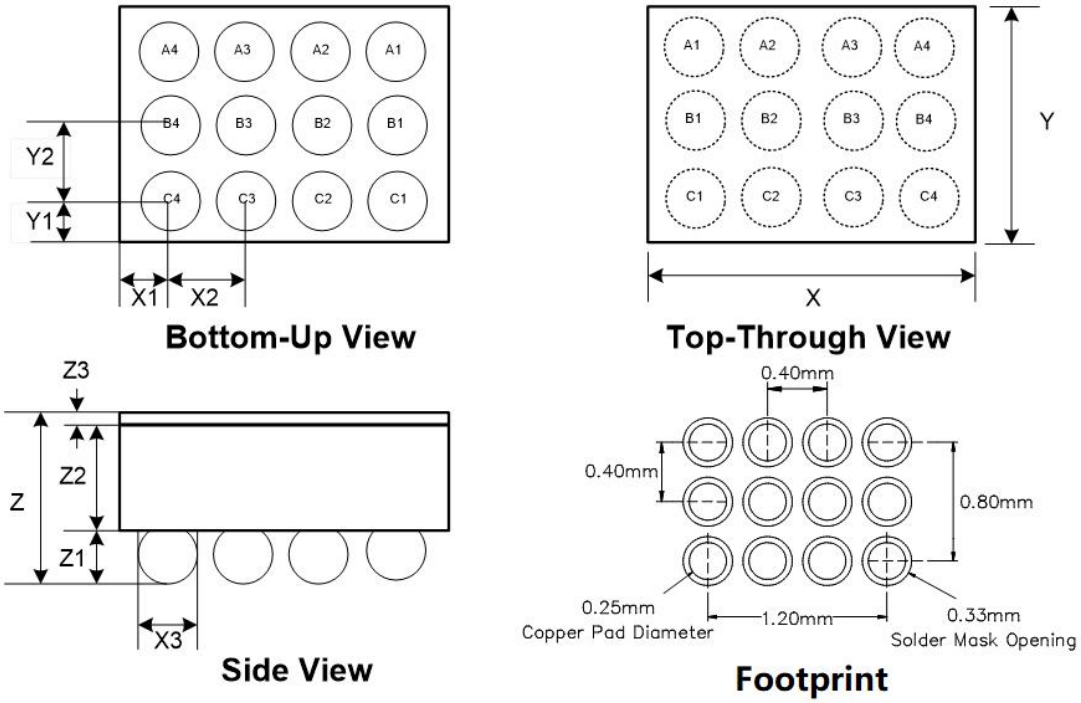


Fig-7 Package Outline Dimensions

Symbol	Dimensions In Millimeter		
	Min.	Typ.	Max.
X	1.58	1.6	1.62
Y	1.18	1.2	1.22
X1		0.20	
X2		0.40	
X3	0.21	0.23	0.25
Y1		0.20	
Y2		0.40	
Z	0.525	0.575	0.625
Z1	0.165	0.185	0.205
Z2	0.340	0.365	0.390
Z3	0.020	0.025	0.030

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