



Description

The HXY8810ES uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V.

General Features

$V_{DS} = 20V, I_D = 7A$

$R_{DS(ON)} < 20m\Omega @ V_{GS}=4.5V$

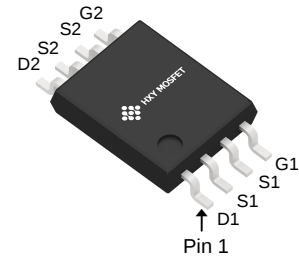
$R_{DS(ON)} < 28m\Omega @ V_{GS}=2.5V$

ESD Rating: 2000V HBM

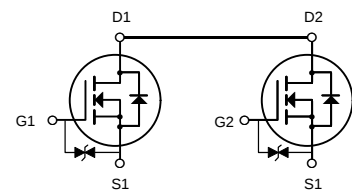
Application

Battery protection

Load switch Power management



TSSOP-8



Dual N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HXY8810ES	TSSOP-8	8810 XXX YYYY	5000

Absolute Maximum Ratings($T_A=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Drain Current-Continuous@ Current-Pulsed	7	A
I_{DM}		25	A
P_D	Maximum Power Dissipation	1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	83	$^{\circ}C/W$



Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 4.5V, V_{DS}=0V$			± 200	nA
		$V_{GS}=\pm 10V, V_{DS}=0V$			± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6	0.75	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=6.5A$		14	20	m Ω
		$V_{GS}=4V, I_D=6A$		16	22	m Ω
		$V_{GS}=3.1V, I_D=5.5A$		19	26	m Ω
		$V_{GS}=2.5V, I_D=5.5A$		24	28	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=6.5A$		6.6		S
Input Capacitance	C_{iss}	$V_{DS}=8V, V_{GS}=0V,$ $F=1.0MHz$		650		PF
Output Capacitance	C_{oss}			360		PF
Reverse Transfer Capacitance	C_{rss}			154		PF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, I_D=1A$ $V_{GS}=4.5V, R_{GEN}=6\Omega$		11	22	nS
Turn-on Rise Time	t_r			12	28	nS
Turn-Off Delay Time	$t_{d(off)}$			35	73	nS
Turn-Off Fall Time	t_f			33	65	nS
Total Gate Charge	Q_g	$V_{DS}=10V, I_D=7A,$ $V_{GS}=4.5V$		11	16	nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			3.2		nC
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=1.5A$		0.84	1.2	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production testing.



Typical Electrical and Thermal Characteristics

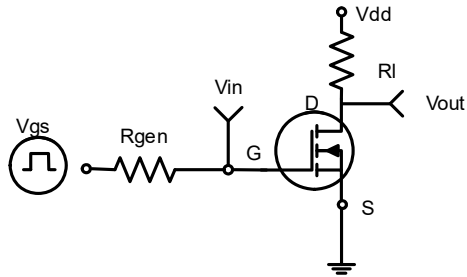


Figure 1: Switching Test Circuit

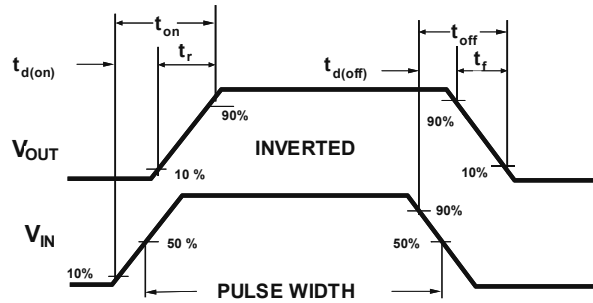


Figure 2: Switching Waveforms

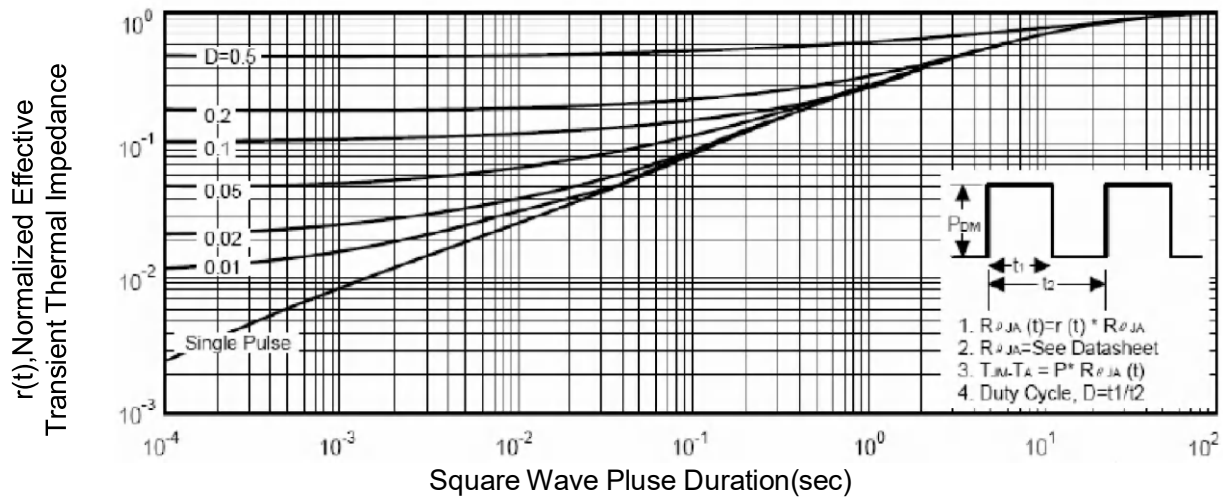
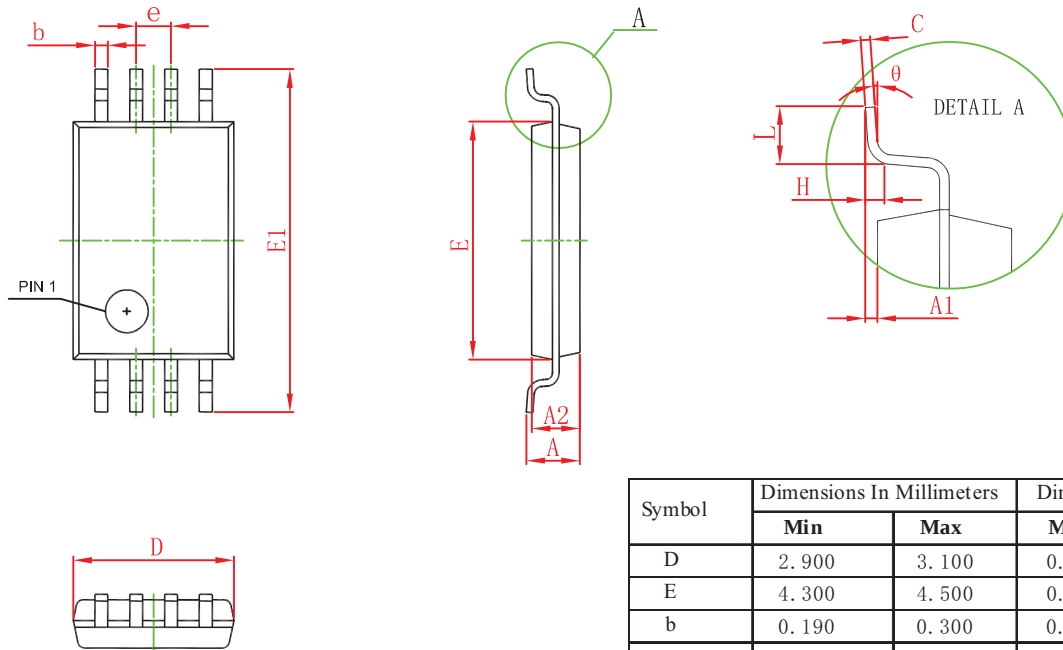


Figure 3 Normalized Maximum Transient Thermal Impedance

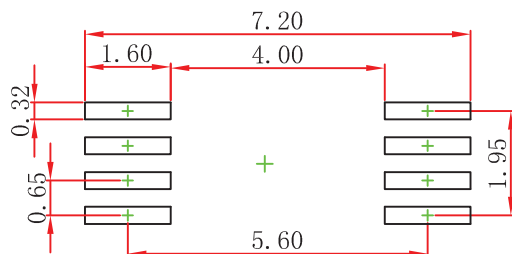


TSSOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

TSSOP-8 Suggested Pad Layout



- Note:
- 1.Controlling dimension:in millimeters.
 - 2.General tolerance:±0.05mm.
 - 3.The pad layout is for reference purposes only.



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