



Description

The HXY8810AES uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V.

General Features

$V_{DS} = 20V, I_D = 8A$

$R_{DS(ON)} < 13m\Omega @ V_{GS}=4.5V$

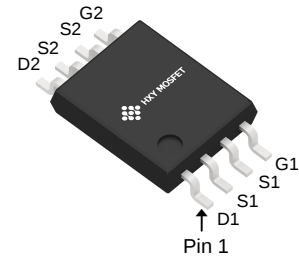
$R_{DS(ON)} < 16m\Omega @ V_{GS}=2.5V$

ESD Rating: 2000V HBM

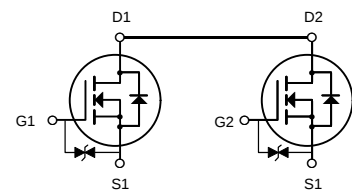
Application

Battery protection

Load switch Power management



TSSOP-8



Dual N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HXY8810AES	TSSOP-8	8810 XXX YYYY	5000

Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 10	V
I_D	Drain Current-Continuous@ Current-Pulsed	8	A
I_{DM}		24	A
P_D	Maximum Power Dissipation	1.23	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	83	$^{\circ}C/W$



Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V$, $I_D=3.5A$		11.5	13	$m\Omega$
		$V_{GS}=2.5V$, $I_D=3.5A$		14.5	16	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	0.5	---	1.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 8V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=3.5A$	---	20	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V$, $V_{GS}=4.5V$, $I_D=7A$	---	11.3	---	nC
Q_{gs}	Gate-Source Charge		---	1.89	---	
Q_{gd}	Gate-Drain Charge		---	3.56	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V$, $V_{GS}=4.5V$, $R_G=3.3\Omega$ $I_D=3.5A$	---	8	---	ns
T_r	Rise Time		---	17	---	
$T_{d(off)}$	Turn-Off Delay Time		---	27	---	
T_f	Fall Time		---	8.8	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	955	---	pF
C_{oss}	Output Capacitance		---	200	---	
C_{rss}	Reverse Transfer Capacitance		---	150	---	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	7	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Notes :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150^oC junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics

Figure1: Output Characteristics

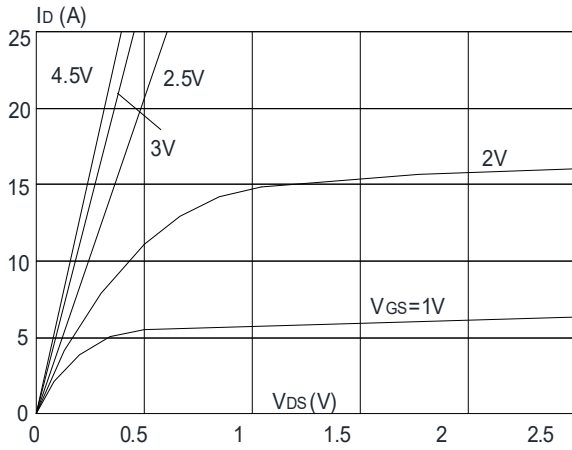


Figure 2: Typical Transfer Characteristics

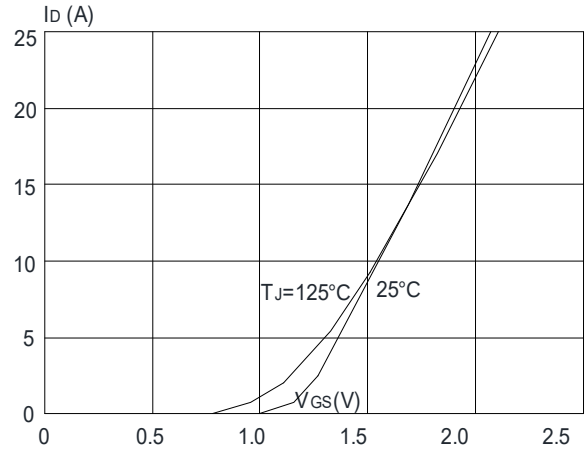


Figure 3: On-resistance vs. Drain Current

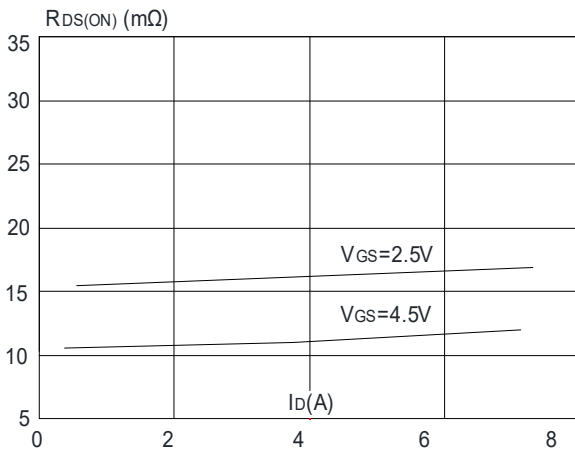


Figure 4: Body Diode Characteristics

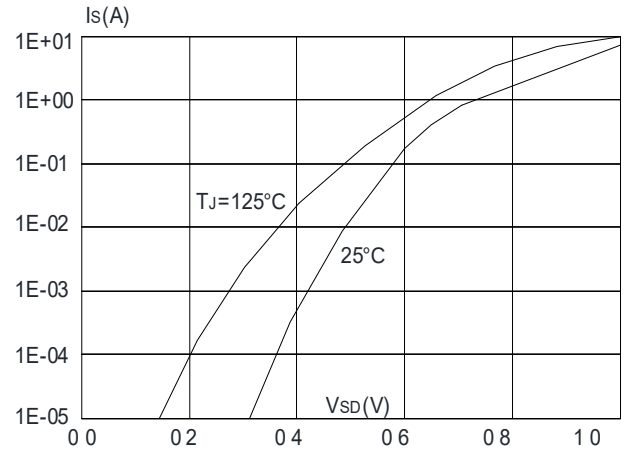


Figure 5: Gate Charge Characteristics

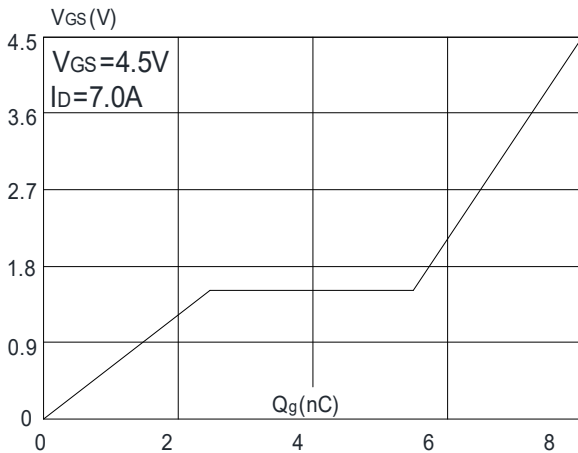


Figure 6: Capacitance Characteristics

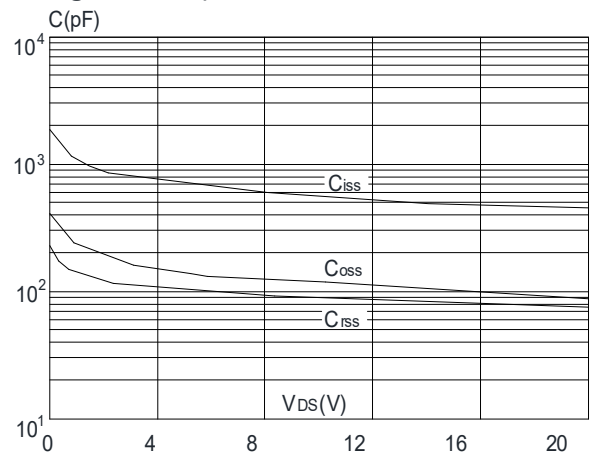




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

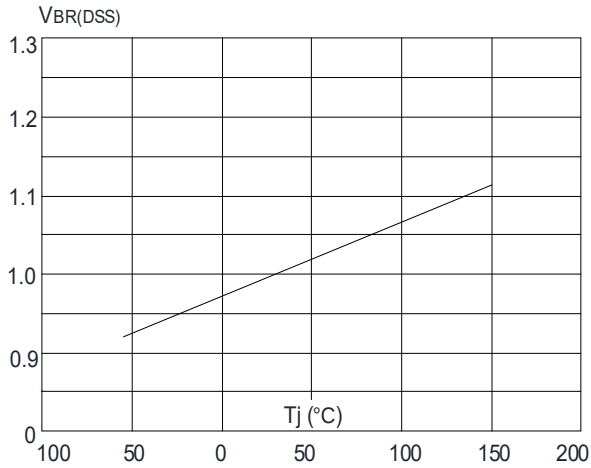


Figure 8: Normalized on Resistance vs. Junction Temperature

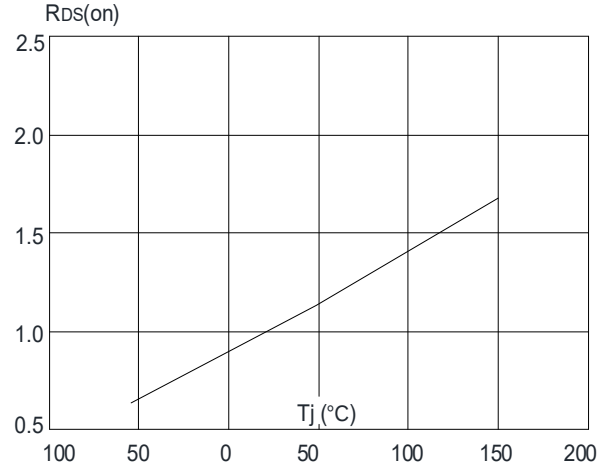


Figure 9: Maximum Safe Operating Area

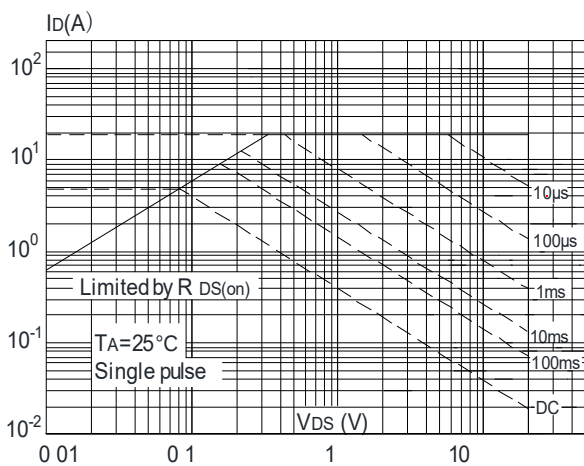


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

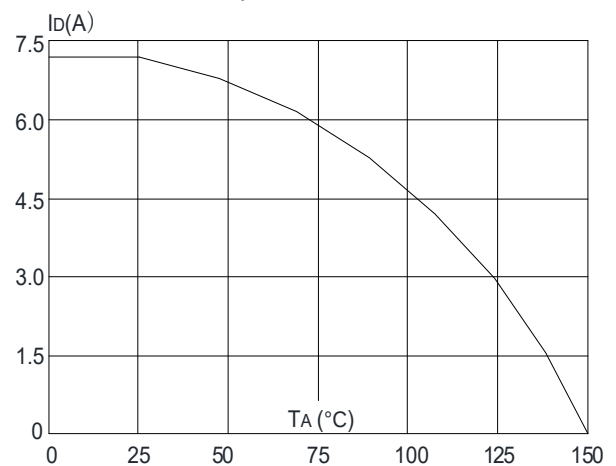
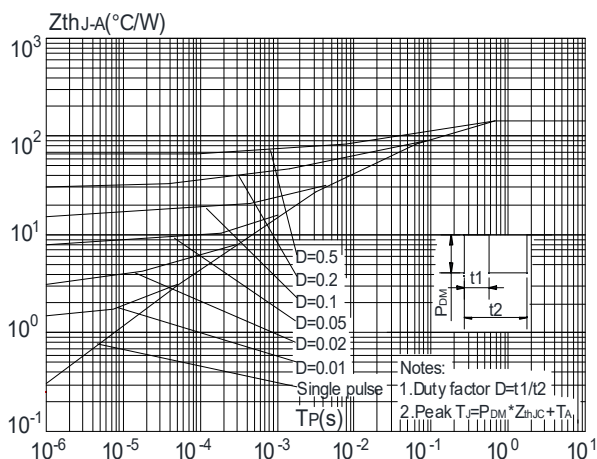
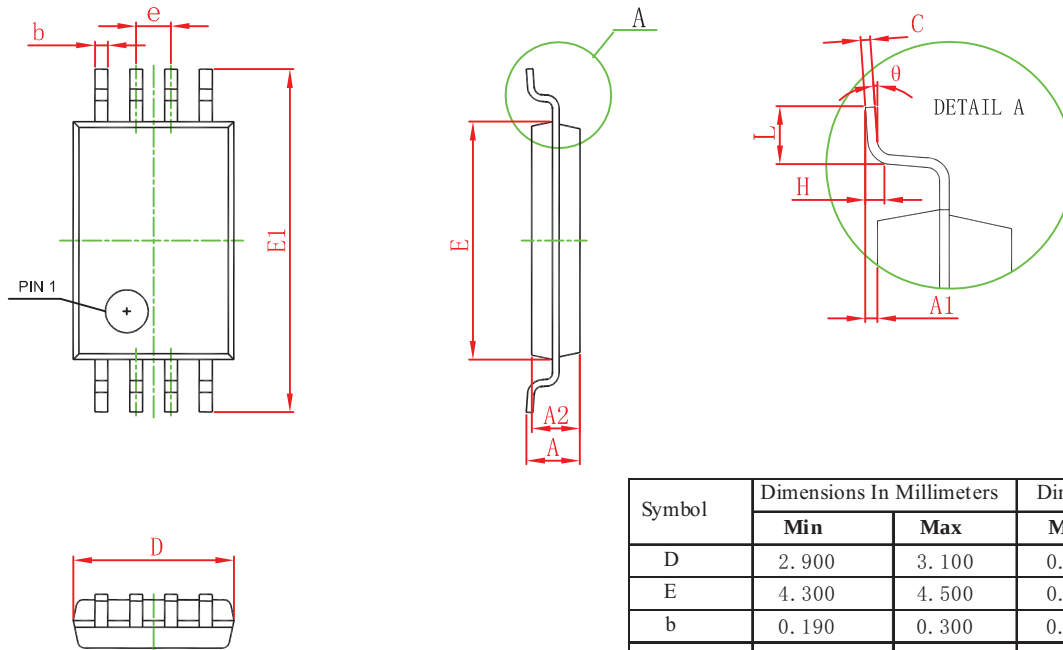


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



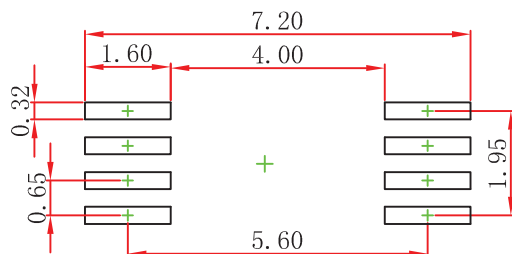


TSSOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

TSSOP-8 Suggested Pad Layout



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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