



Description

The HIRFZ44NSTRLPBF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

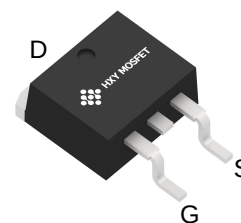
$V_{DS} = 55V$ $I_D = 49A$

$R_{DS(ON)} < 13m\Omega @ V_{GS}=10V$

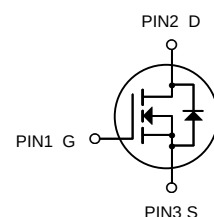
Application

Switching application

Power Management for Inverter Systems.



TO-263
(D2PAK)



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Units/Tube)
HIRFZ44NSTRLPBF	TO-263(D2PAK)	HXY MOSFET	50

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{DS}	Drain-Source Voltage	55	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current-Continuous	49	A
$I_D (100^\circ C)$	Drain Current-Continuous($T_C=100^\circ C$)	35	A
I_{DM}	Pulsed Drain Current	160	A
P_D	Maximum Power Dissipation	94	W
E_{AR}	Repetitive Avalanche Energy	9.4	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance,Junction-to-Case ^(Note 2)	1.5	$^\circ C/W$



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.058		V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		10	13	m Ω	$V_{GS} = 10V, I_D = 25A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	19			S	$V_{DS} = 25V, I_D = 25A$
I_{DSS}	Drain-to-Source Leakage Current			25	μA	$V_{DS} = 55V, V_{GS} = 0V$
				250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage			-100		$V_{GS} = -20V$
Q_g	Total Gate Charge			63	nC	$I_D = 25A$
Q_{gs}	Gate-to-Source Charge			14		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge			23		$V_{GS} = 10V$, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time		12		ns	$V_{DD} = 28V$
t_r	Rise Time		60			$I_D = 25A$
$t_{d(off)}$	Turn-Off Delay Time		44			$R_G = 12\Omega$
t_f	Fall Time		45			$V_{GS} = 10V$, See Fig. 10
L_S	Internal Source Inductance		7.5		nH	Between lead, and center of die contact
C_{iss}	Input Capacitance		1470		pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance		360			$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance		88			$f = 1.0MHz$, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy		530	150	mJ	$I_{AS} = 25A, L = 0.47mH$

Source-Drain Ratings and Characteristics

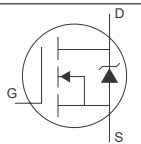
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			49	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)			160		
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$
t_{rr}	Reverse Recovery Time		63	95	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
Q_{rr}	Reverse Recovery Charge		170	260	nC	$di/dt = 100A/\mu s$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.48mH$
 $R_G = 25\Omega$, $I_{AS} = 25A$. (See Figure 12)
- ③ $I_{SD} \leq 25A$, $di/dt \leq 230A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ This is a typical value at device destruction and represents operation outside rated limits.
- ⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.



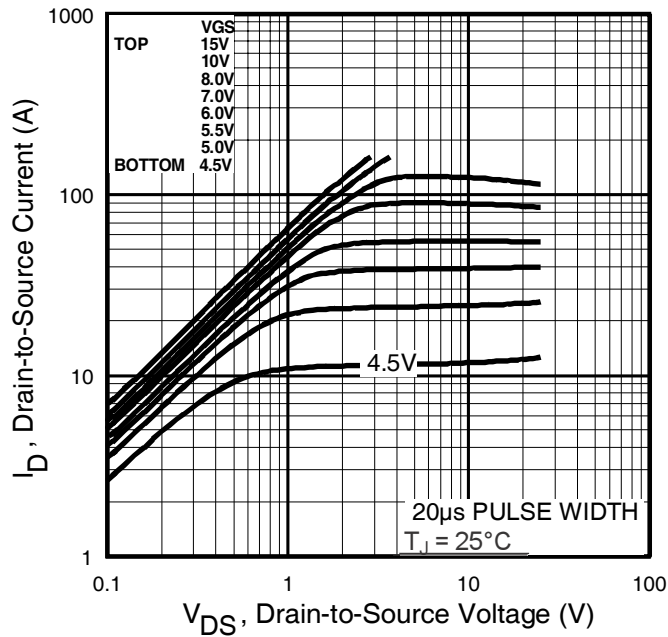


Fig 1. Typical Output Characteristics

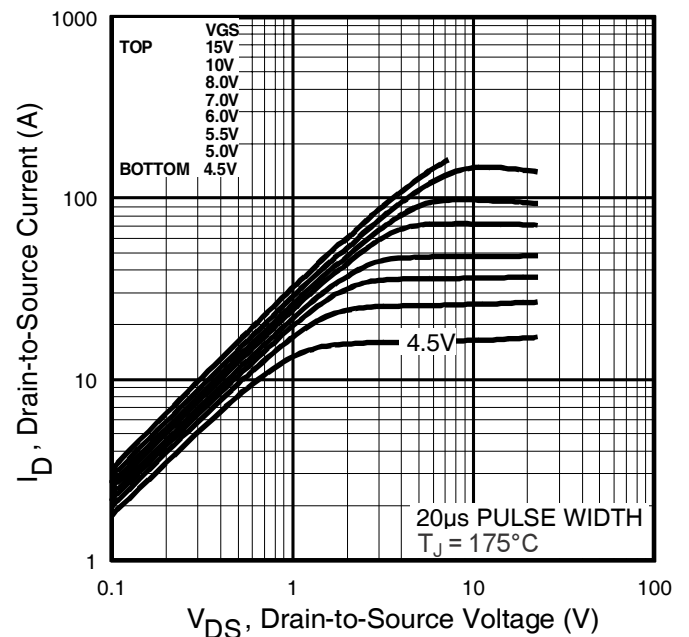


Fig 2. Typical Output Characteristics

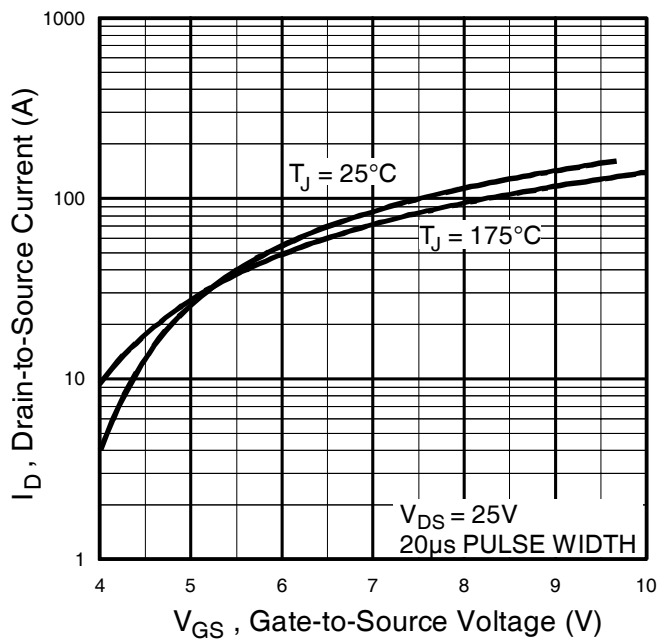


Fig 3. Typical Transfer Characteristics

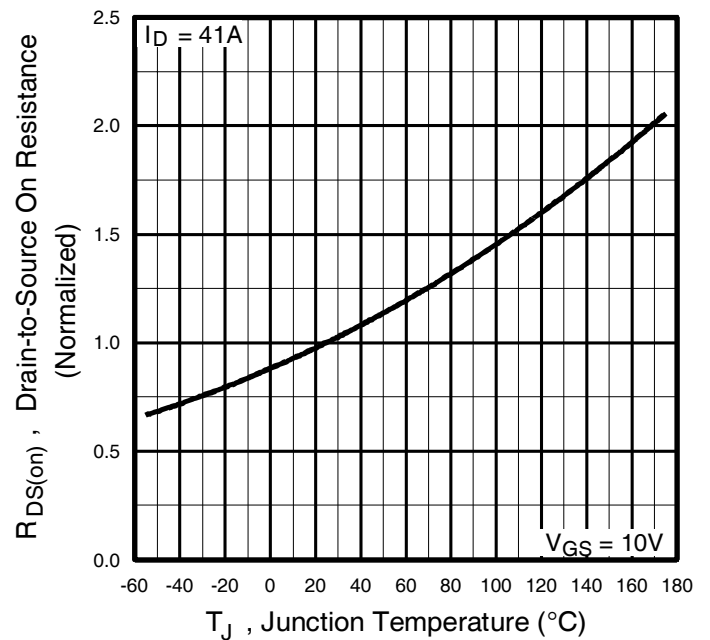


Fig 4. Normalized On-Resistance Vs. Temperature

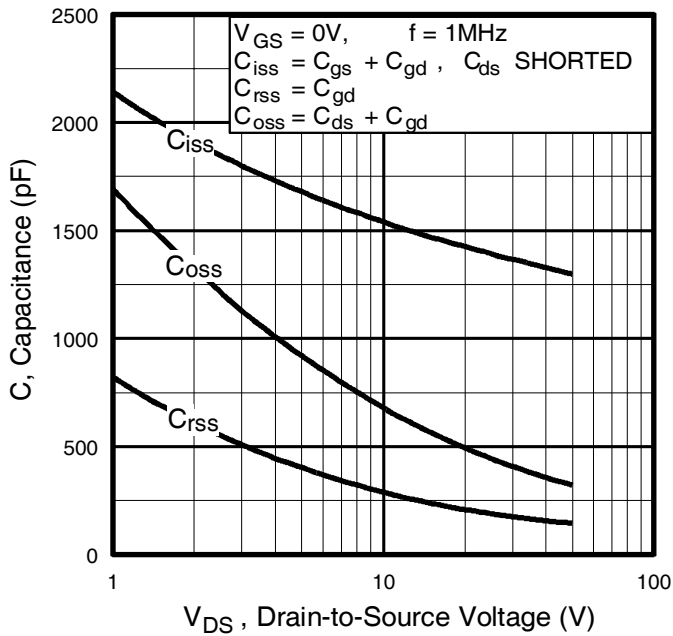


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

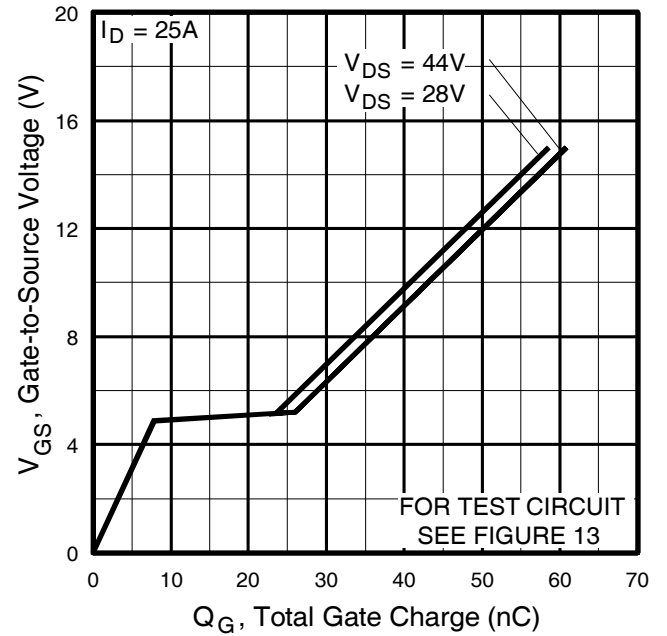


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

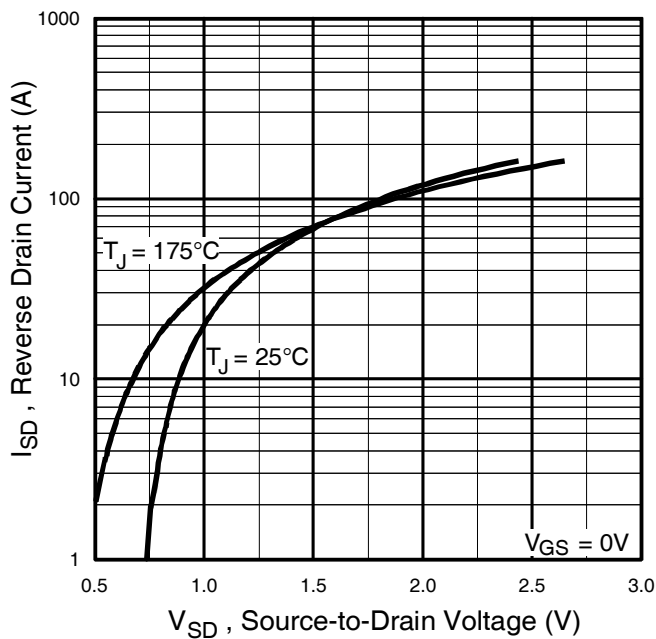


Fig 7. Typical Source-Drain Diode Forward Voltage

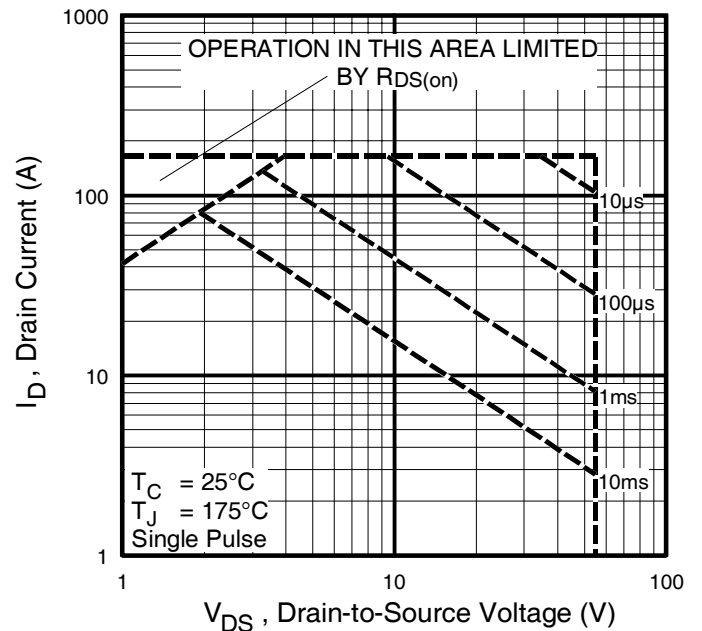


Fig 8. Maximum Safe Operating Area

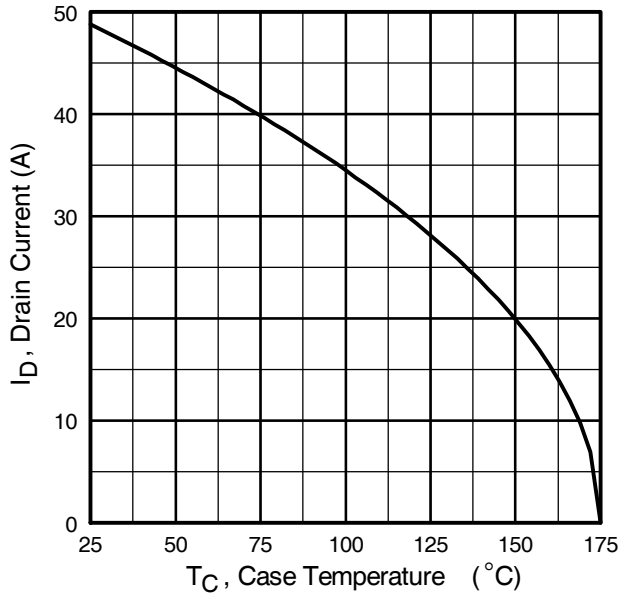


Fig 9. Maximum Drain Current Vs. Case Temperature

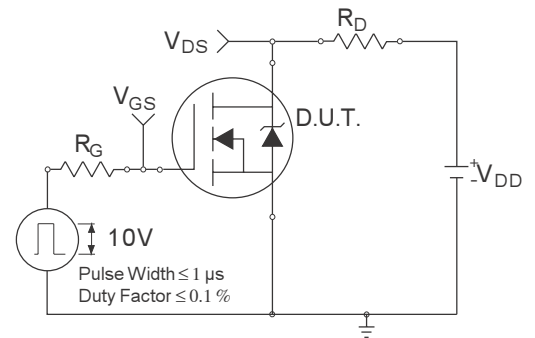


Fig 10a. Switching Time Test Circuit

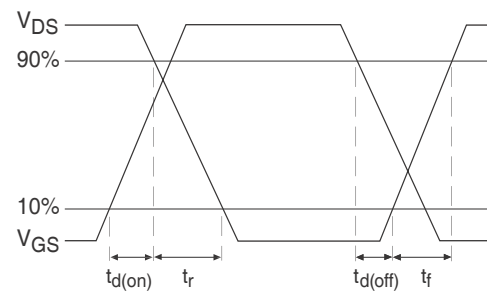


Fig 10b. Switching Time Waveforms

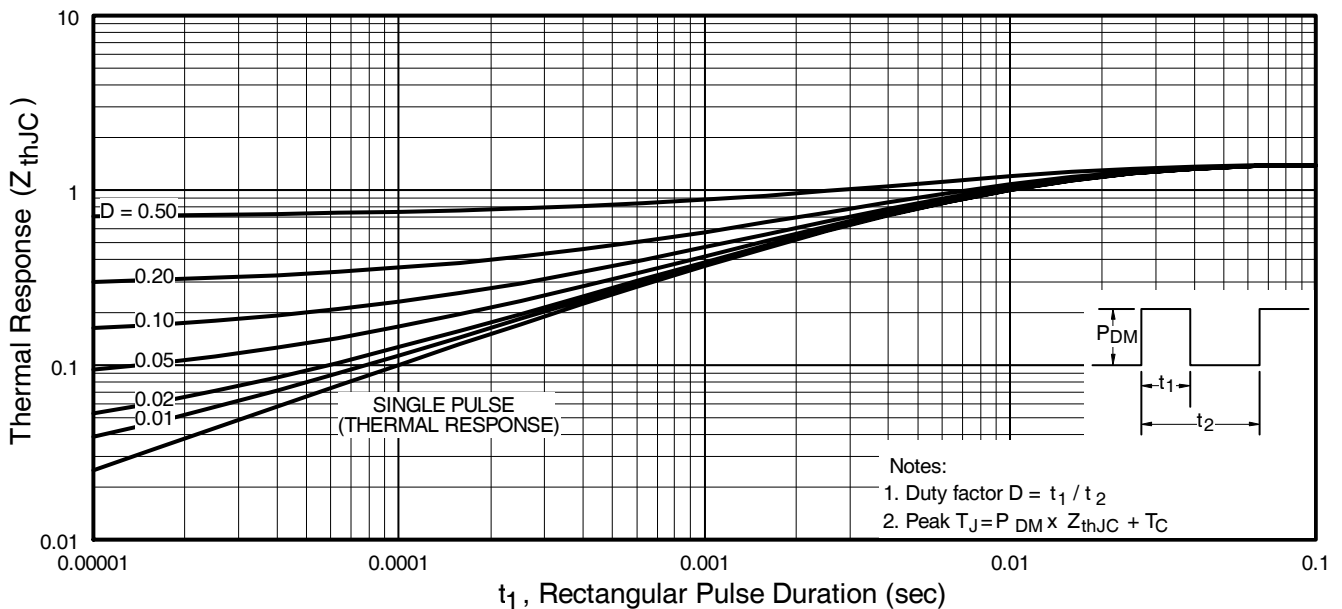


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

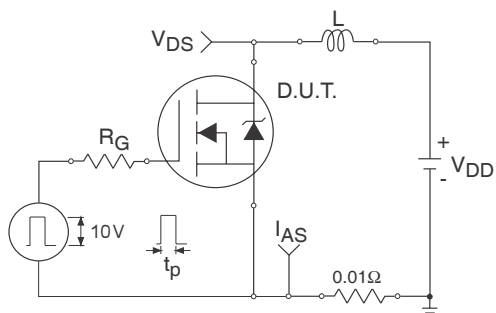


Fig 12a. Unclamped Inductive Test Circuit

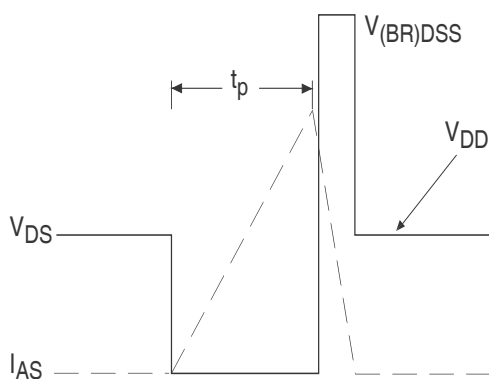


Fig 12b. Unclamped Inductive Waveforms

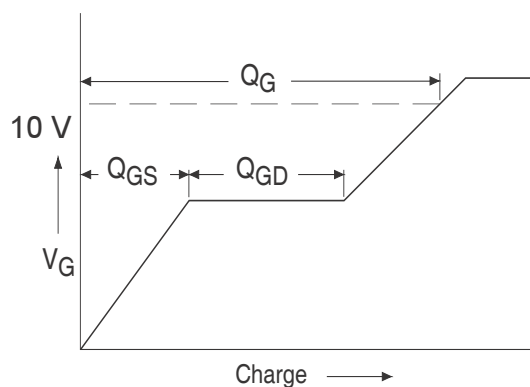


Fig 13a. Basic Gate Charge Waveform

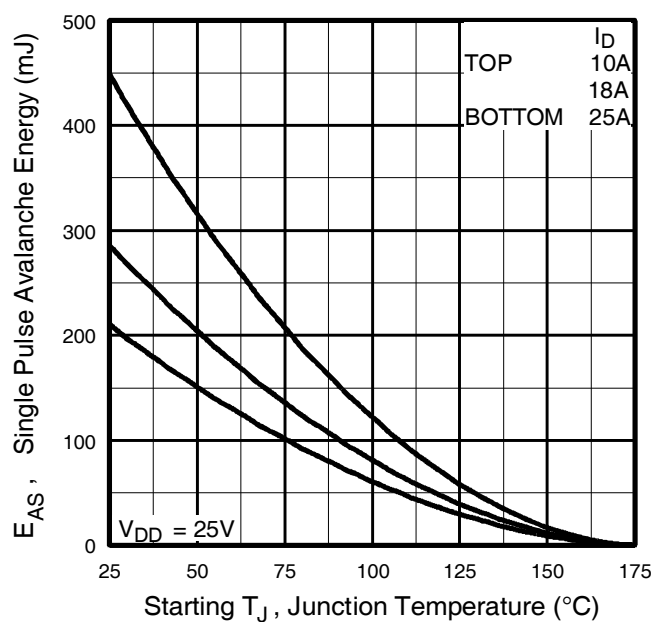


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

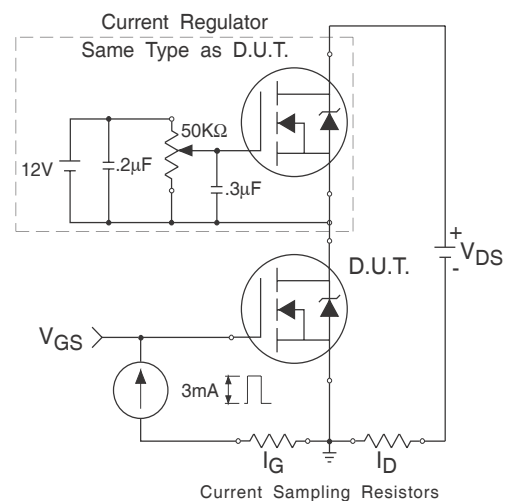


Fig 13b. Gate Charge Test Circuit

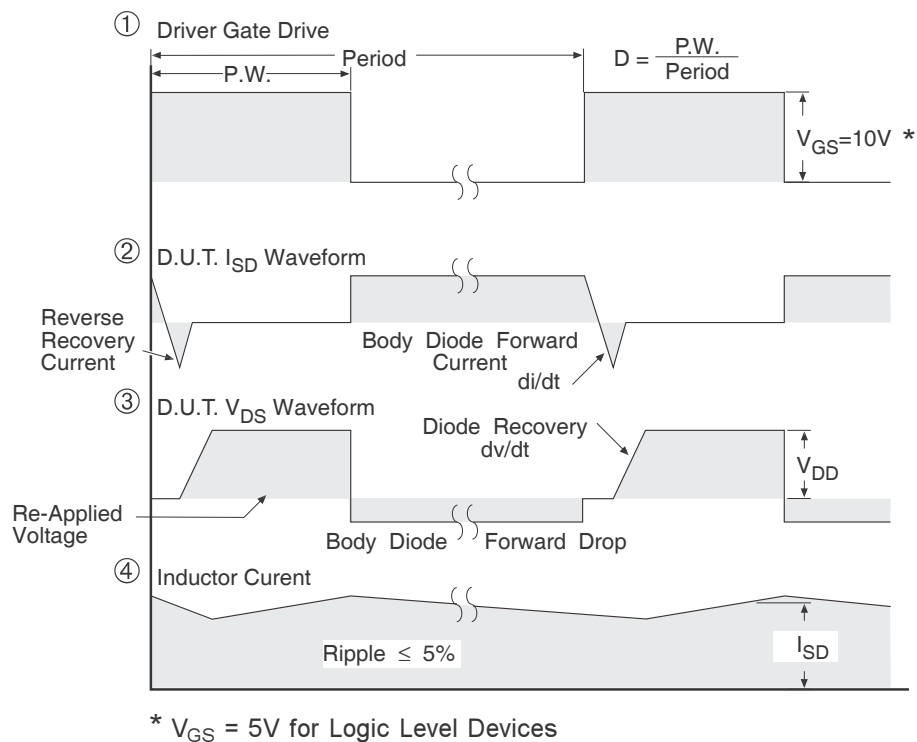
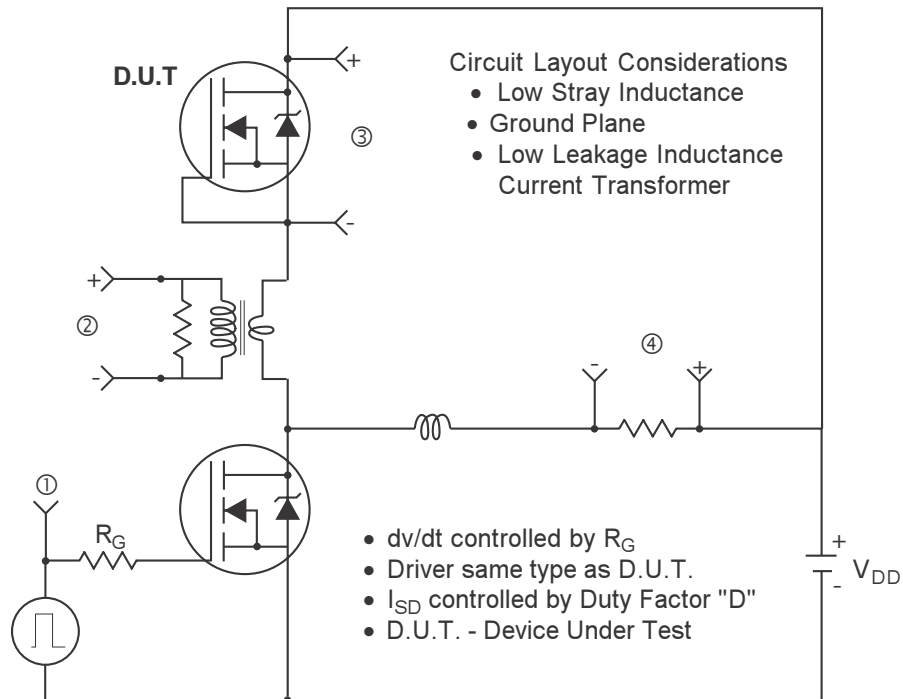
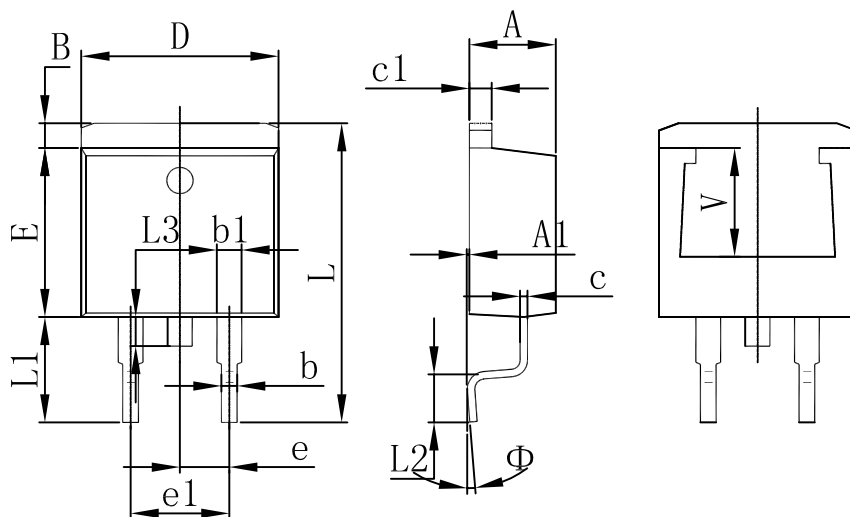


Fig 14. For N-Channel HEXFETS



TO-263(DPAK)Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	0.000	0.150	0.000	0.006
B	1.120	1.420	0.044	0.056
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
L	14.940	15.500	0.588	0.610
L1	4.950	5.450	0.195	0.215
L2	2.340	2.740	0.092	0.108
L3	1.300	1.700	0.051	0.067
Φ	0°	8°	0°	8°
V	5.600 REF.		0.220REF.	



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