

#### **Description**

The DMP3010LK3-13 uses advanced trench technology to provide excellent R<sub>DS(ON)</sub>, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

# G TO-252-2L (TO-252(DPAK)

#### **General Features**

 $V_{DS} = -30V I_{D} = 80 A$ 

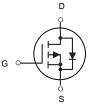
 $R_{DS(ON)}$  < 8.8 m $\Omega$  @  $V_{GS}$ =10V

### **Application**

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

## **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
DMP3010LK3-13	TO-252-2L(TO-252(DPAK)	HXY MOSFET	2500

## Absolute Maximum Ratings (T<sub>c</sub>=25 °C unless otherwise noted)

Symbol	Parameter	Rating	
V <sub>D</sub> s	Drain-Source Voltage	-30	٧
Vgs	Gate-Source Voltage	Gate-Source Voltage ±25	
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-80	Α
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup> -42	
Ідм	Pulsed Drain Current <sup>2</sup>	Pulsed Drain Current <sup>2</sup> -172	
EAS	Single Pulse Avalanche Energy <sup>3</sup>	31	mJ
las	Avalanche Current	-25	А
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	31.2	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>4</sup>	2	W
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
R <sub>0</sub> JA	Thermal Resistance Junction-Ambient <sup>1</sup>	43	°C/W
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	4	°C/W



#### Electrical Characteristics Tc = 25°C, unless otherwise noted

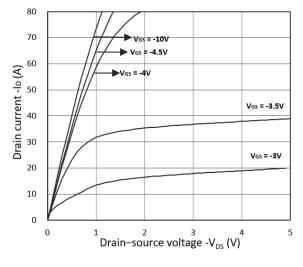
Parameter		Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Drain-Source Breakdown Voltage		V <sub>(BR)DSS</sub>	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V	
Gate-body Leakage current	Gate-body Leakage current		V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA	
Zero Gate Voltage Drain Current	TJ=25°C		\\ - 24\\ \\ - 0\\	-	-	-1	μА	
	TJ=55°C	- I <sub>DSS</sub>	$V_{DS} = -24V, V_{GS} = 0V$	-	-	-5		
Gate-Threshold Voltage		V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1.0	-1.6	-2.5	V	
Drain-Source On-Resistance <sup>2</sup>		-	V <sub>GS</sub> = -10V, I <sub>D</sub> = -12A	-	5.5	8.8		
		R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -8A	-	9	14	mΩ	
Forward Transconductance		<b>g</b> fs	V <sub>DS</sub> = -5V, I <sub>D</sub> = -20A	-	28	-	S	
Input Capacitance		Ciss		-	4320	-	pF	
Output Capacitance		Coss	V <sub>DS</sub> = -15V, V <sub>GS</sub> =0V, f =1MHz	-	529	-		
Reverse Transfer Capacitance		C <sub>rss</sub>		-	487	-		
Gate Resistance		$R_g$	$V_{DS}$ = 0V, $V_{GS}$ = 0V, f=1.0MHz	-	4.0	-	Ω	
Total Gate Charge		Qg		-	45	-	nC	
Gate-Source Charge		Qgs	$V_{GS} = -10V, V_{DS} = -15V,$ $I_{D} = -15A$	-	8.5	-		
Gate-Drain Charge		Q <sub>gd</sub>		-	12.8	-		
Turn-On Delay Time		t <sub>d(on)</sub>		-	18.9	-	nS	
Rise Time		t <sub>r</sub>	$V_{GS} = -10V, V_{DD} = -15V,$	-	15.7	-		
Turn-Off Delay Time		t <sub>d(off)</sub>	$R_G = 2.5\Omega$ , $I_D = -15A$	-	64.8	-		
Fall Time		t <sub>f</sub>		-	36.5	-		
Diode Forward Voltage <sup>2</sup>		VsD	I <sub>S</sub> = -1A, V <sub>GS</sub> = 0V	-	-	-1	V	
Continuous Source Current <sup>1,5</sup>		Is	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current		-	-80	Α	

#### Note:

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ = -25V,  $V_{GS}$ = -10V, L= 0.1mH,  $I_{AS}$ = -25A
- 4.The power dissipation is limited by 150  $^{\circ}\text{C}$  junction temperature
- 5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



#### **Typical Characteristics**



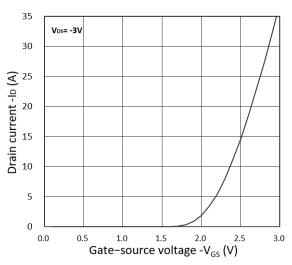


Figure 1. Output Characteristics

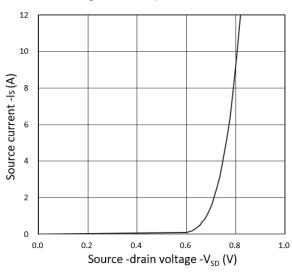


Figure 2. Transfer Characteristics

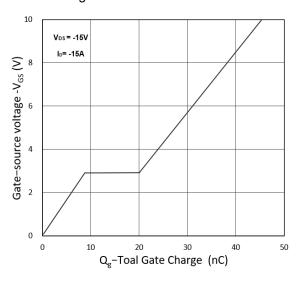


Figure 3. Forward Characteristics of Reverse

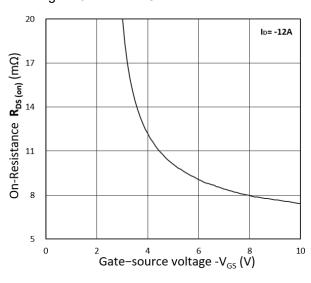


Figure 4. Gate Charge Characteristics

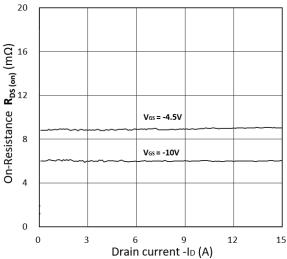


Figure 5. RDS(on) vs. VGS

Figure 6. R<sub>DS(on)</sub> vs. I<sub>D</sub>

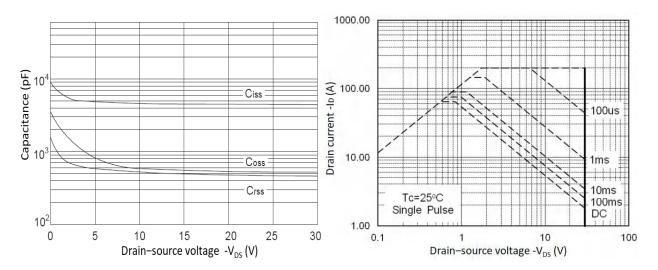


Figure 7. Capacitance Characteristics

Figure 8. Safe Operating Area

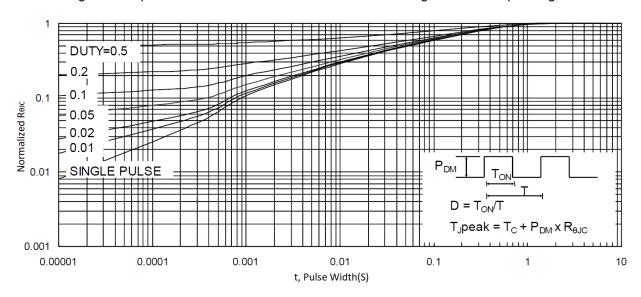


Figure 9. Normalized Maximum Transient Thermal Impedance

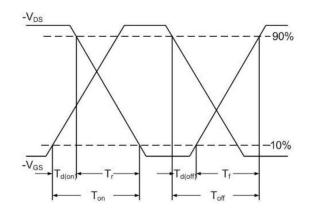


Figure 10. Switching Time Waveform

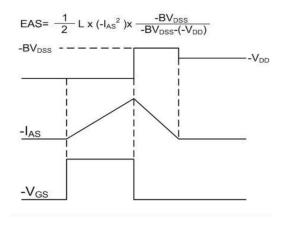


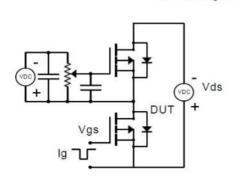
Figure 11. Unclamped Inductive Switching

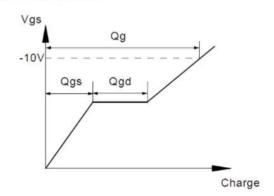
Waveform



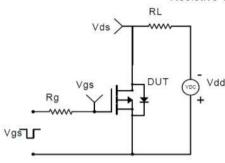
## **Test Circuit**

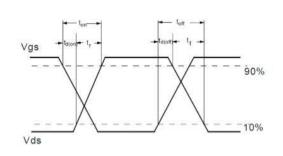
#### Gate Charge Test Circuit & Waveform



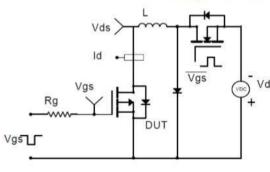


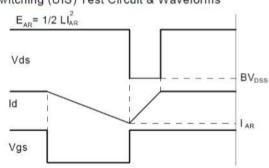
Resistive Switching Test Circuit & Waveforms



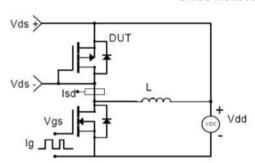


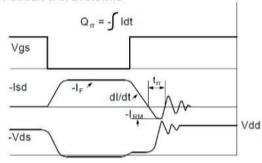
### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





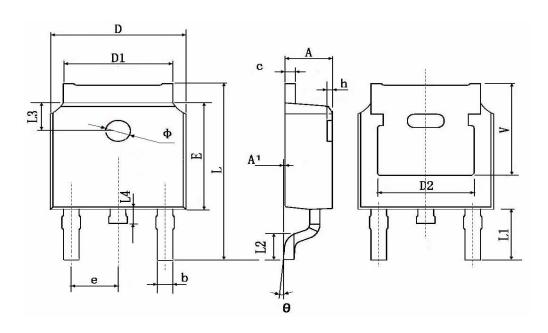
#### Diode Recovery Test Circuit & Waveforms







## TO-252-2L(TO-252(DPAK)) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min.	Max.	Min.	Max.	
А	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.660	0.860	0.026	0.034	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2	4.830 TYP.		0.190 TYP.		
Е	6.000	6.200	0.236	0.244	
е	2.186	2.386	0.086	0.094	
L	9.800	10.400	0.386	0.409	
L1	2.900 TYP.		0.114 TYP.		
L2	1.400	1.700	0.055	0.067	
L3	1.600 TYP.		0.063 TYP.		
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.350 TYP.		0.211 TYP.		

#### P-Channel Enhancement Mode MOSFET

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