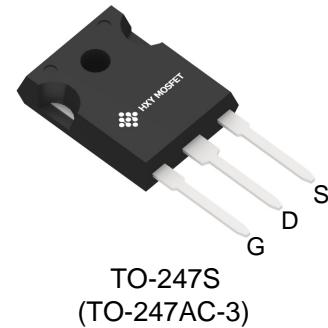




Description

The HXY14N50MPS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 500V$ $I_D = 14A$

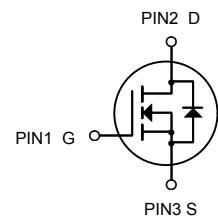
$R_{DS(ON)} < 0.5\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HXY14N50MPS	TO-247S(TO-247AC-3)	IRFP450 XXXX	30

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	14	A
$I_D @ T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8.7	A
I_{DM}	Pulsed Drain Current	56	A
EAS	Single Pulse Avalanche Energy	760	mJ
I_{AS}	Avalanche Current	8.7	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation	190	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
R_{thJA}	Maximum Junction-to-Ambient	40	°C/W
R_{thJC}	Maximum Junction-to-Case (Drain)	0.65	°C/W



Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	500	-	-	V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.63	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.0	-	4.0	V	
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	25	μA	
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125°C	-	-	250		
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 8.4 A ^b	-	0.43	0.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V	I _D = 8.4 A ^b	9.3	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	2600	-	pF	
Output Capacitance	C _{oss}		-	720	-		
Reverse Transfer Capacitance	C _{rss}		-	340	-		
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 14 A, V _{DS} = 400 V, see fig. 6 and 13 ^b	-	-	150	nC
Gate-Source Charge	Q _{gs}			-	-	20	
Gate-Drain Charge	Q _{gd}			-	-	80	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 14 A, R _G = 6.2 Ω, R _D = 17 Ω, see fig. 10 ^b	-	17	-	ns	
Rise Time	t _r		-	47	-		
Turn-Off Delay Time	t _{d(off)}		-	92	-		
Fall Time	t _f		-	44	-		
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact	-	5.0	-	nH	
Internal Source Inductance	L _S		-	13	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode	-	-	14	A	
Pulsed Diode Forward Current ^a	I _{SM}		-	-	56		
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 14 A, V _{GS} = 0 V ^b	-	-	1.4	V	
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 14 A, dI/dt = 100 A/μs ^b	-	540	810	ns	
Body Diode Reverse Recovery Charge	r _{rQ}		-	4.8	7.2	μC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.



Typical Characteristics $T_a = 25^\circ\text{C}$, unless otherwise noted

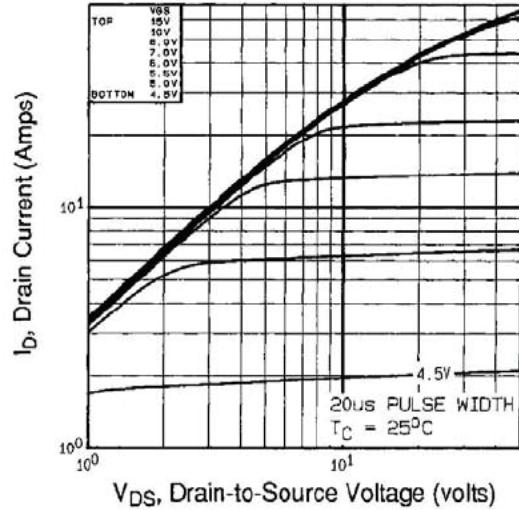


Fig. 1 - Typical Output Characteristics, $T_c = 25^\circ\text{C}$

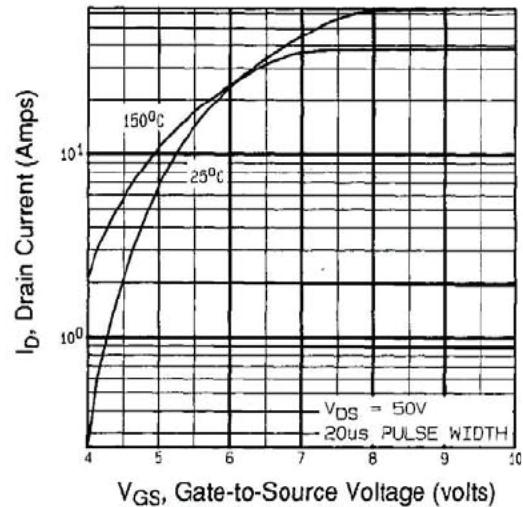


Fig. 3 - Typical Transfer Characteristics

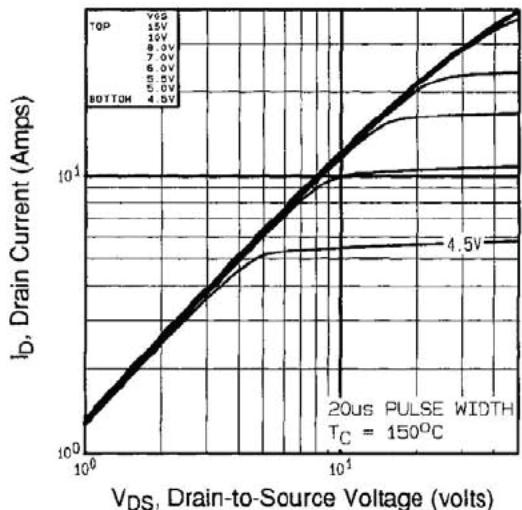


Fig. 2 - Typical Output Characteristics, $T_c = 150^\circ\text{C}$

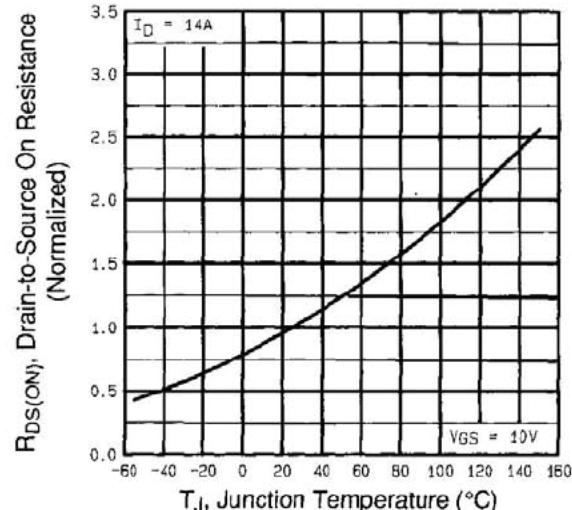


Fig. 4 - Normalized On-Resistance vs. Temperature

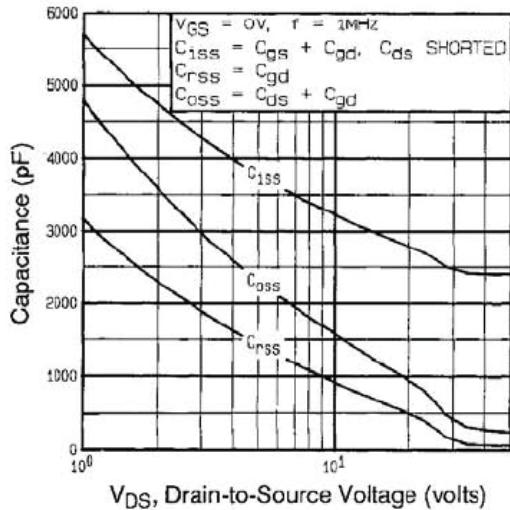


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

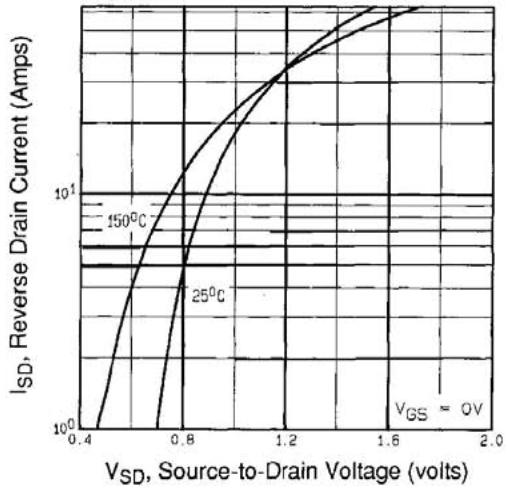


Fig. 7 - Typical Source-Drain Diode Forward Voltage

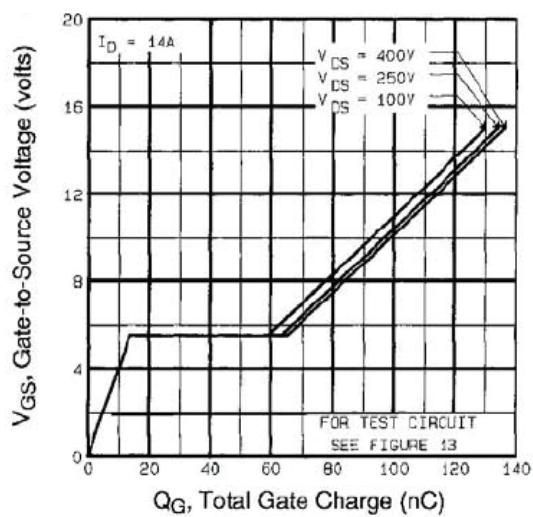


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

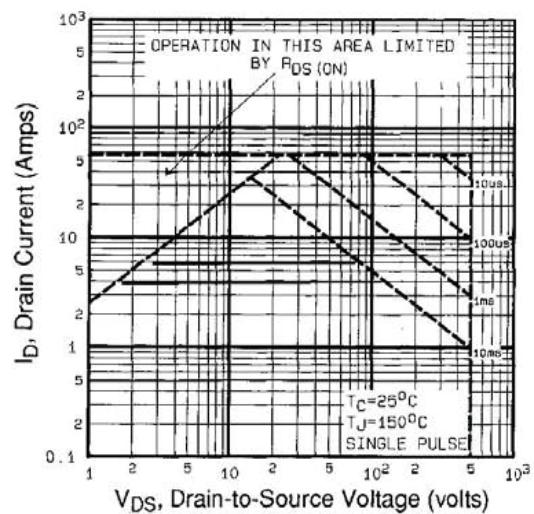


Fig. 8 - Maximum Safe Operating Area

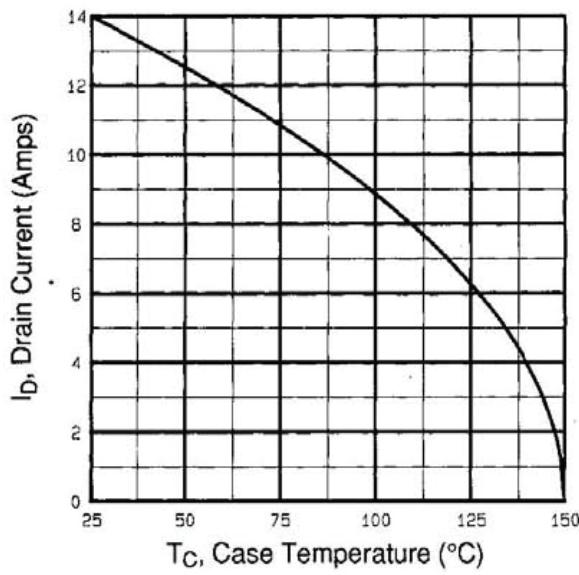


Fig. 9 - Maximum Drain Current vs. Case Temperature

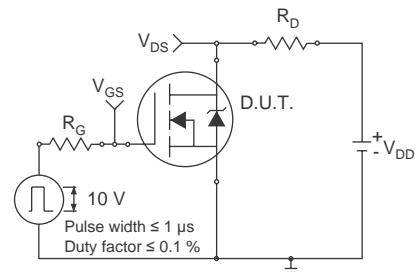


Fig. 10a - Switching Time Test Circuit

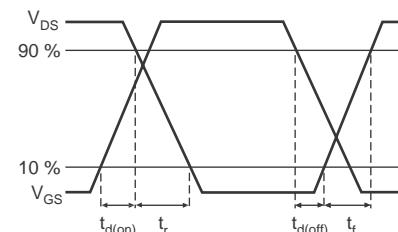


Fig. 10b - Switching Time Waveforms

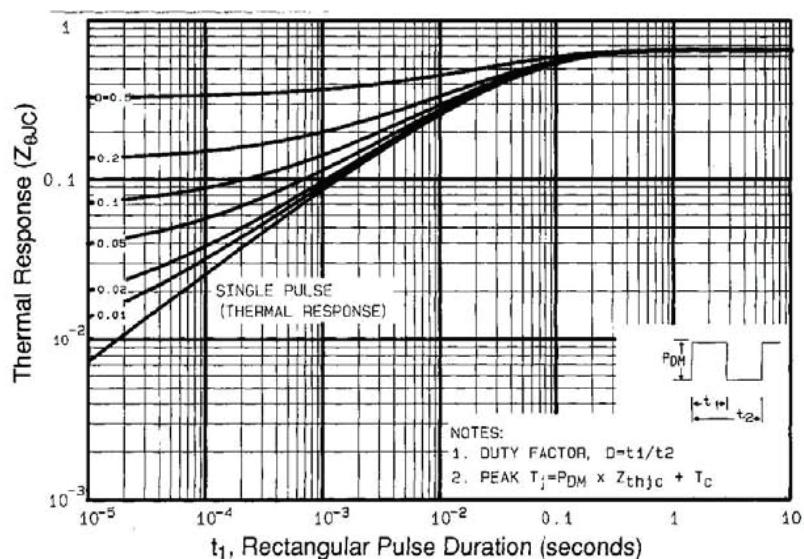


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

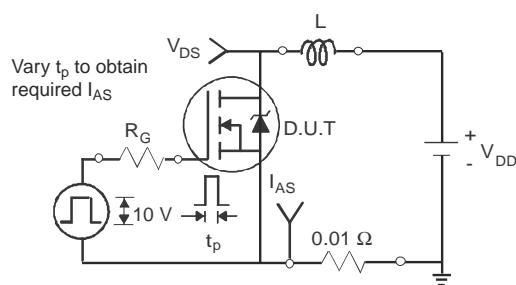


Fig. 12a - Unclamped Inductive Test Circuit

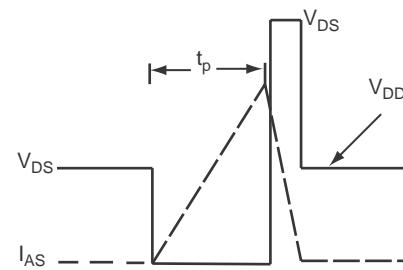


Fig. 12b - Unclamped Inductive Waveforms

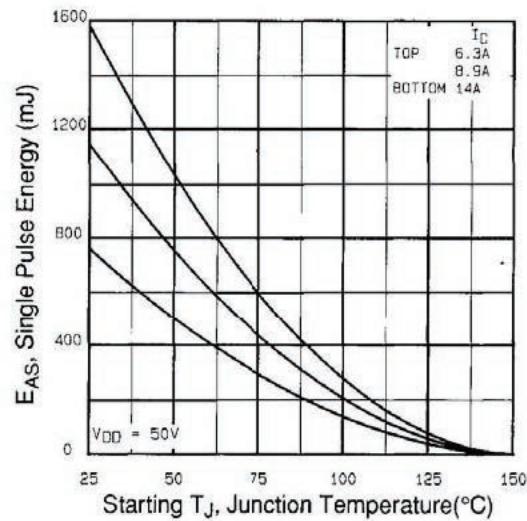


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

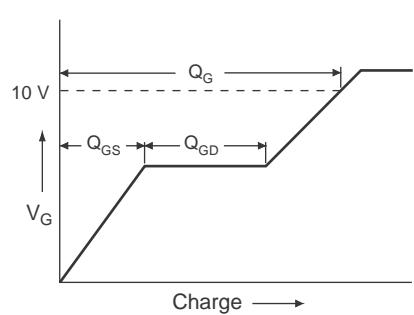


Fig. 13a - Basic Gate Charge Waveform

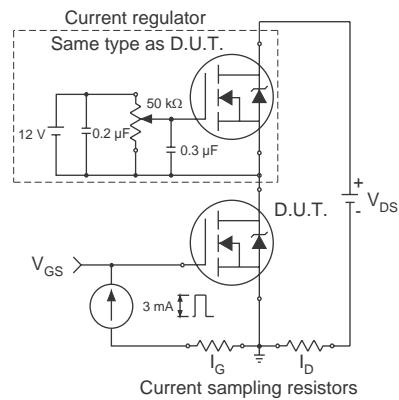
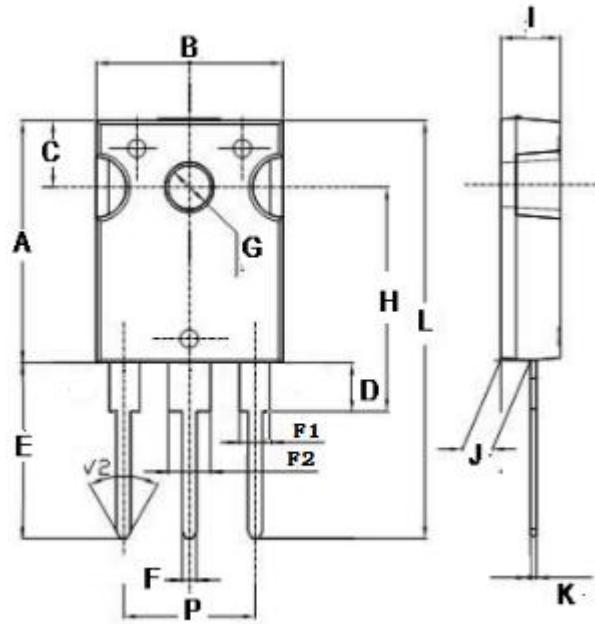


Fig. 13b - Gate Charge Test Circuit



TO-247S(TO-247AC-3) Package Information



Dim	Min	Max
A	20.0	22.0
B	15.5	16.0
C	5.7	6.3
D	4.0	4.4
E	19.0	21.0
F	1.1	1.3
G	3.5	3.8
H	18.3	20.2
I	4.9	5.2
J	2.3	2.5
K	0.55	0.65
L	39.0	42.0
P	10.7	10.9
F1	1.9	2.1
F2	2.9	3.1
mm		



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