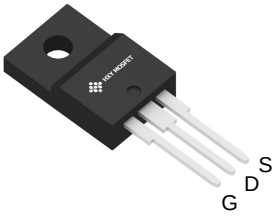
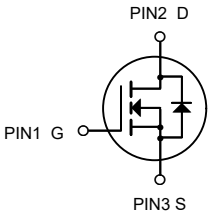
Description

The SMIRF13N50T2TL can be used in various power swithching circuit for system miniaturization and higher efficiency.The package form is TO-220/ TO-220F, which accords with the RoHS standard.



TO-220F



N-Channel MOSFET

General Features

V_{DS} = 500V,I_D =13A
$R_{DS(ON)}$ < 0.48Ω@ V_{GS}=10V

Application

● Power switch circuit of adaptor and charger.

Package Marking and Ordering Information

Product ID	Pack	Marking	Units Tube
SMIRF13N50T2TL	TO-220F	13N50 XXX YYYY	50

Absolute Maximum Ratings@T =25°C(unless otherwise specified)

Symbol	Parameter	Limit	Unit
V_{DSS}	Drain-to-Source Voltage[1]	500	V
V_{GSS}	Gate-to-Source Voltage	±30	
$I_{D\ @\ Tc=100℃}$	Continuous Drain Current @ Tc=100℃	13	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2]	52	
E_{AS}	Single Pulse Avalanche Energy	900	mJ
P_D	Power Dissipation	48	W
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.6	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Electrical Characteristics T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=500V, V_{GS}=0V
		--	--	100		V_{DS}=400V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}==30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	0.40	0.48	Ω	V_{GS}=10V, I_D=6.5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	--	15	--	S	VDS=30V,ID=13A
C_{iss}	Input Capacitance	--	2150	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MH_Z
C_{rss}	Reverse Transfer Capacitance	--	23	--		
C_{oss}	Output Capacitance	--	210	--		
Q_g	Total Gate Charge	--	45	--	nC	V_{DD}=250V, I_D=13A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	10	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	18	--		
$td_{(ON)}$	Turn-on Delay Time	--	15	--	ns	V_{DD}=250V, I_D=13A, V_{GS}=10V Rg=6.1 Ω
t_{rise}	Rise Time	--	25	--		
$td_{(OFF)}$	Turn-Off Delay Time	--	45	--		
t_{fall}	Fall Time	--	35	--		
I_{SD}	Continuous Source Current[2]	--	--	13	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	52		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=13A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	500	--	ns	V_{GS}=0V I_F=13A, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	4.0	--	uC	

Note:

[1] T_J=+25℃ to +150℃
[2] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

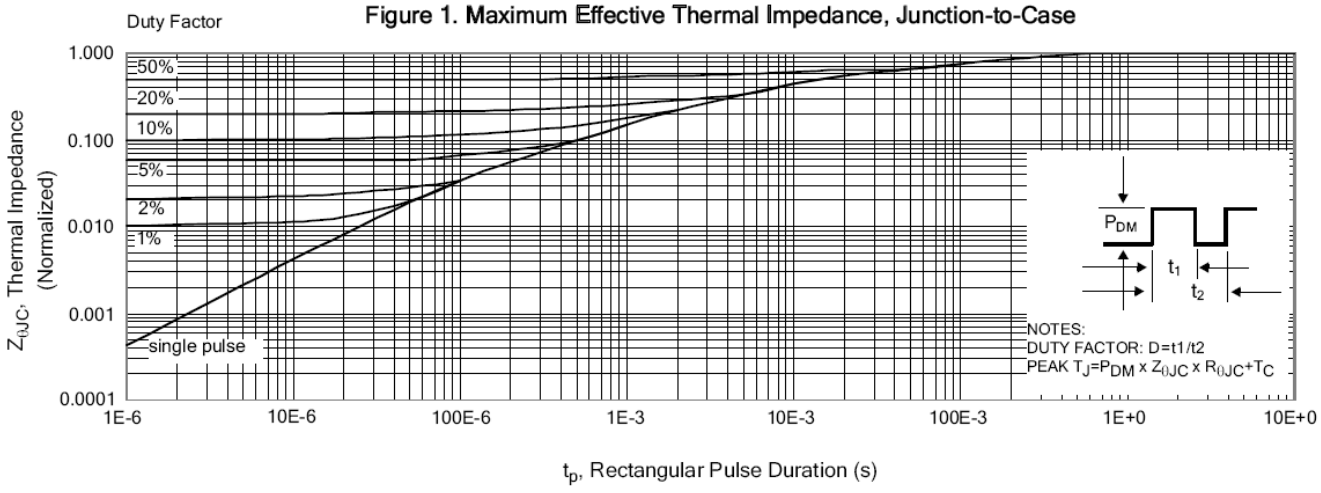


Figure 2. Maximum Power Dissipation vs Case Temperature

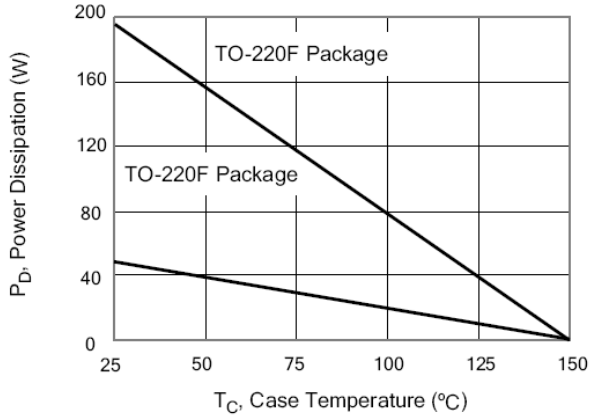


Figure 3. Maximum Continuous Drain Current vs Case Temperature

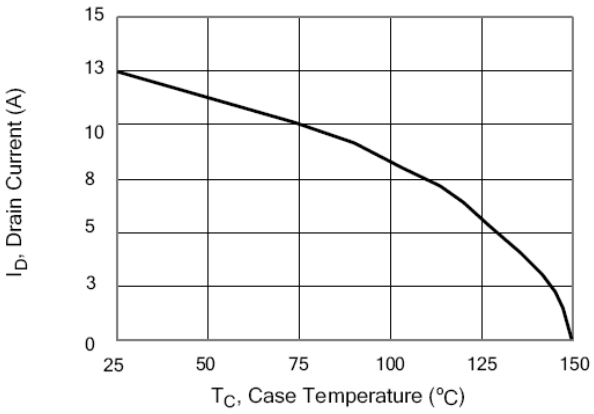


Figure 4. Typical Output Characteristics

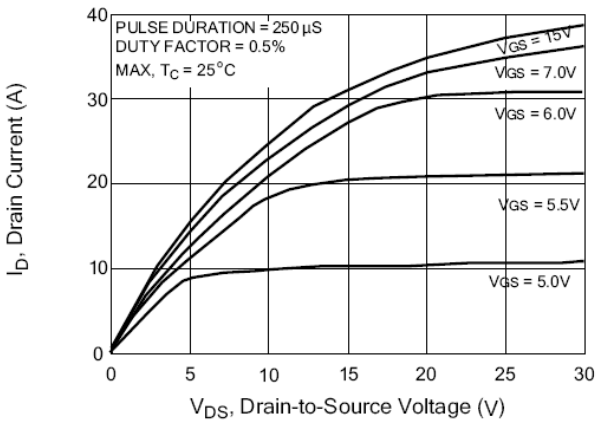


Figure 5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

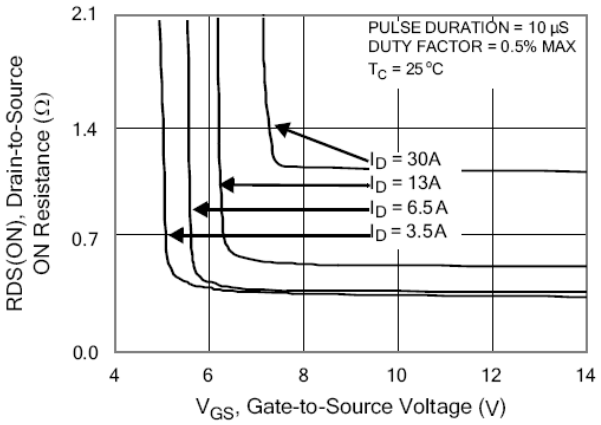


Figure 6. Maximum Peak Current Capability

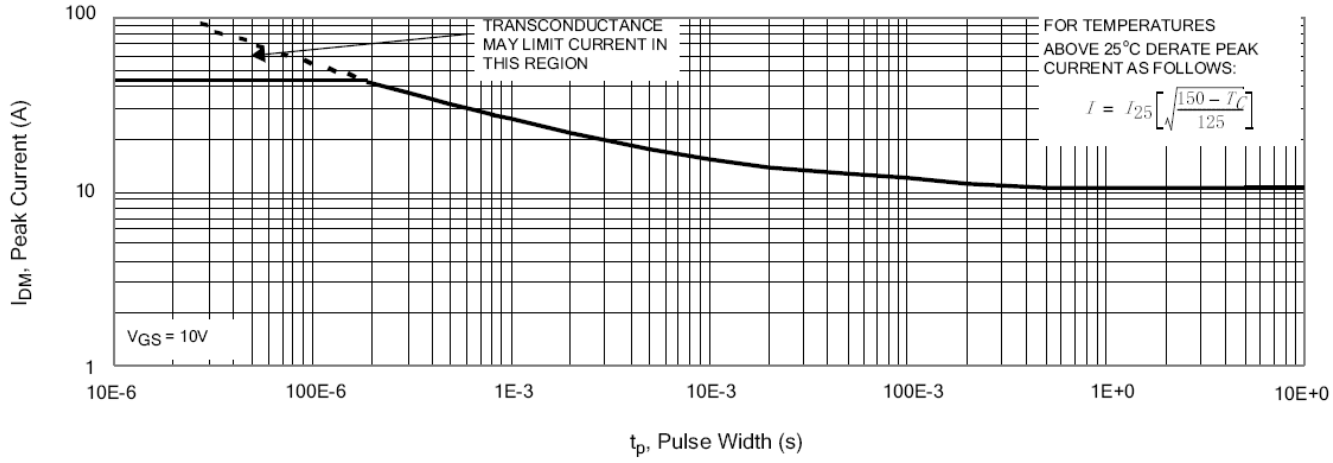


Figure 7. Typical Transfer Characteristics

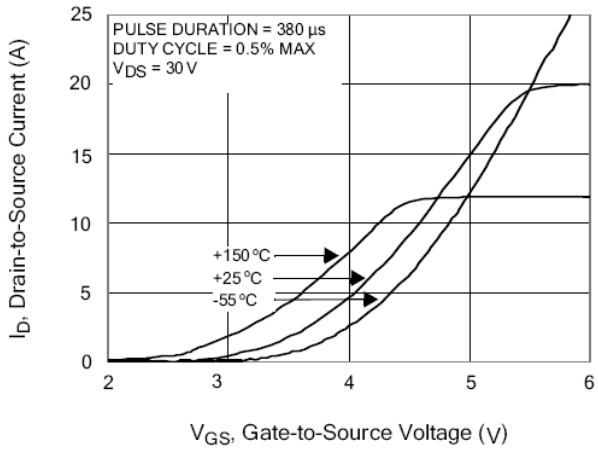


Figure 8. Unclamped Inductive Switching Capability

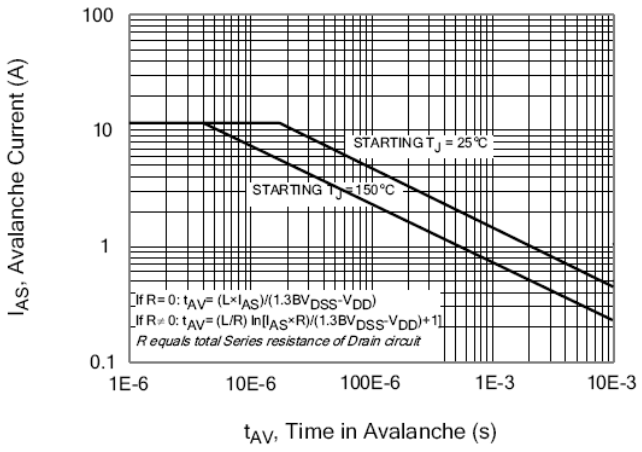


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

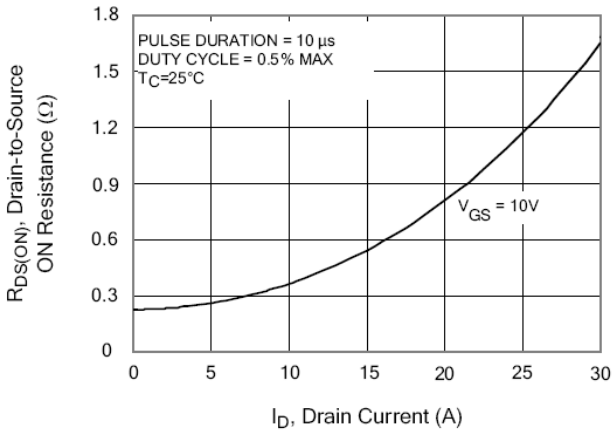
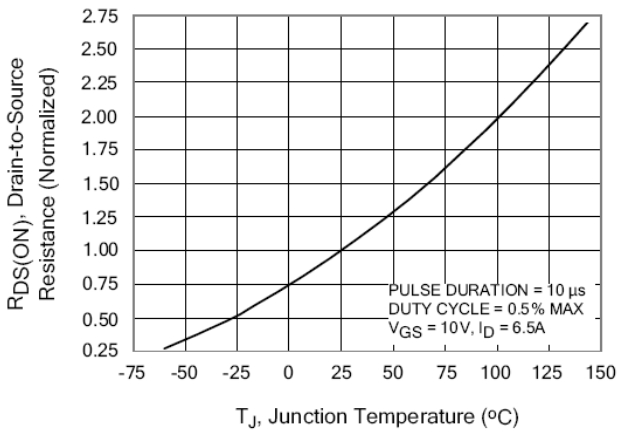


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

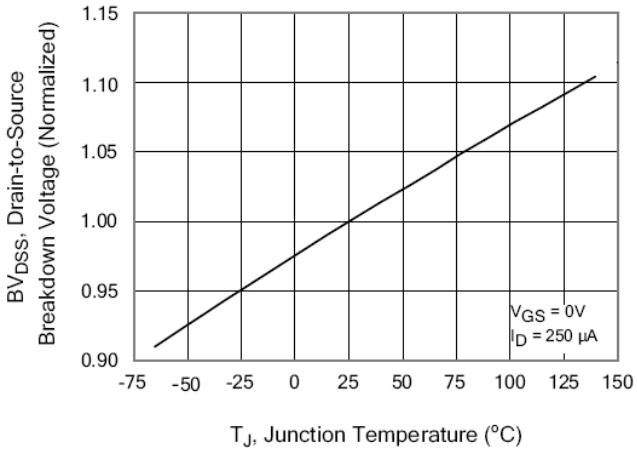


Figure 12. Typical Threshold Voltage vs Junction Temperature

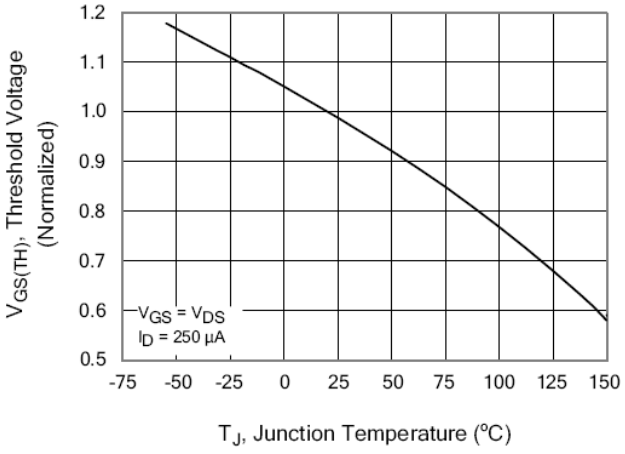


Figure 13. Maximum Forward Bias Safe Operating Area

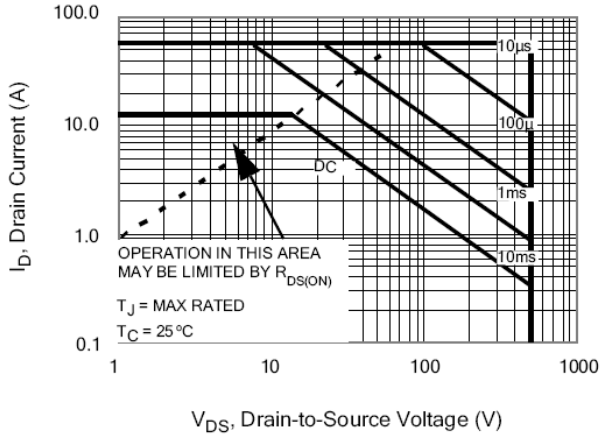


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

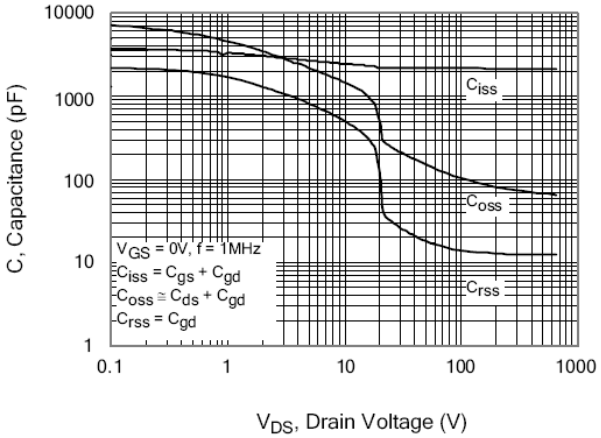


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

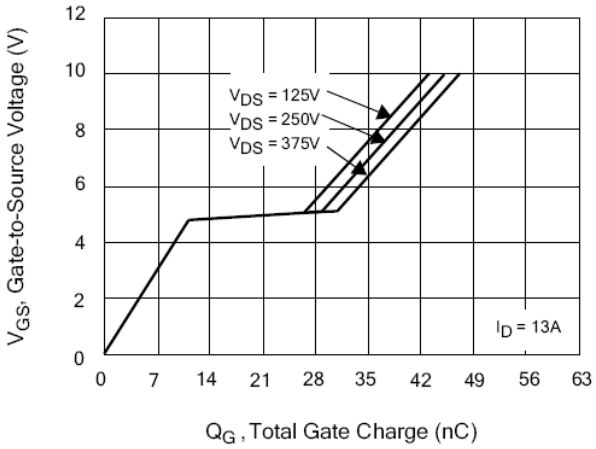
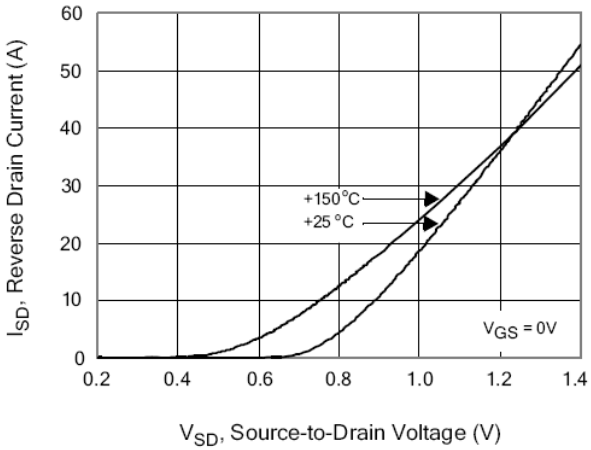


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

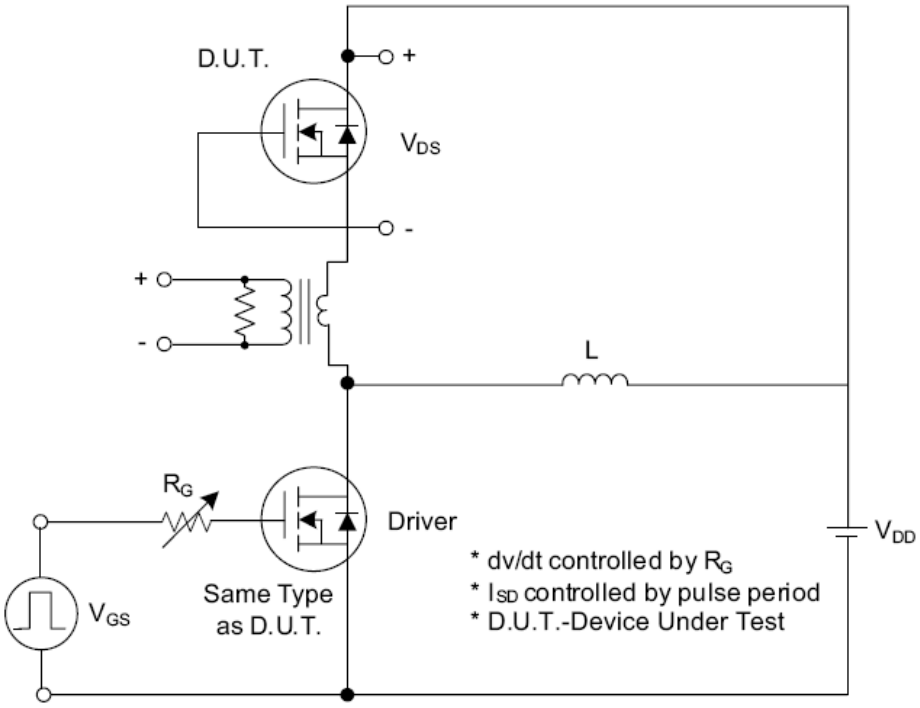


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

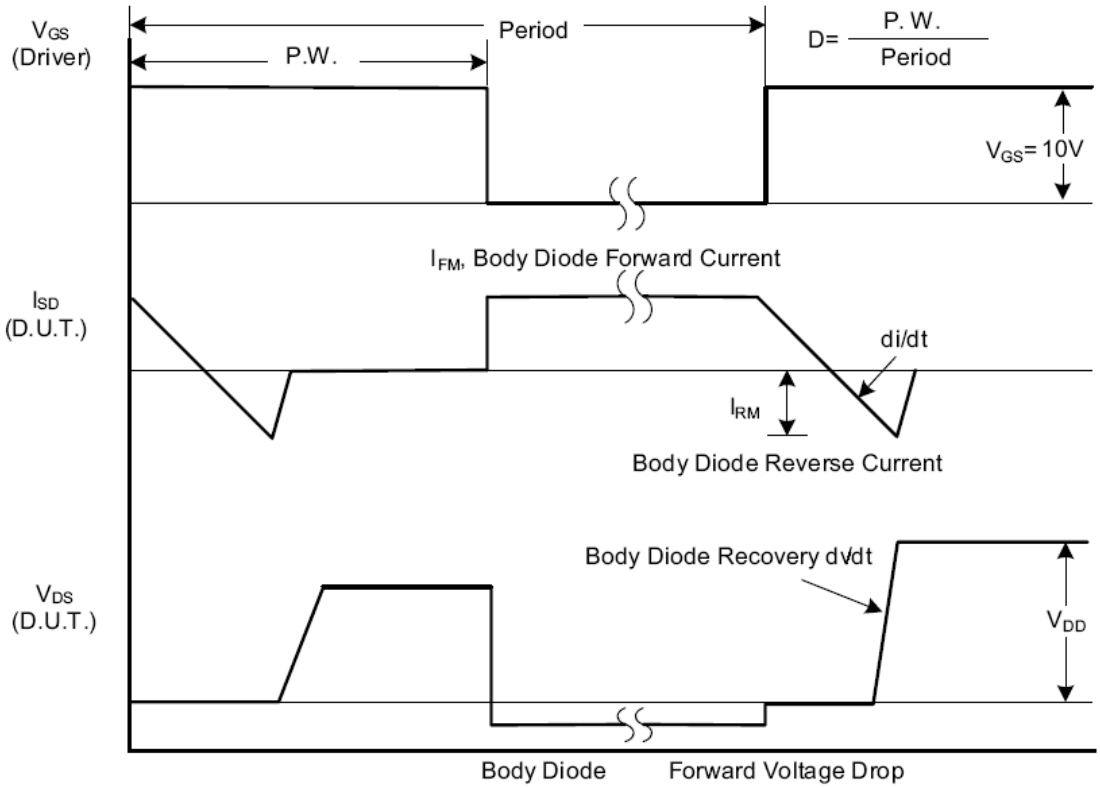


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

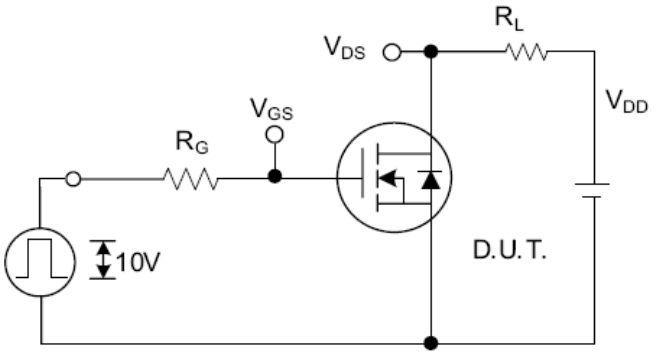


Fig. 2.1 Switching Test Circuit

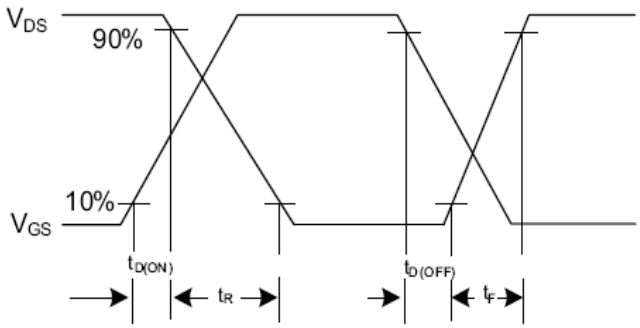


Fig. 2.2 Switching Waveforms

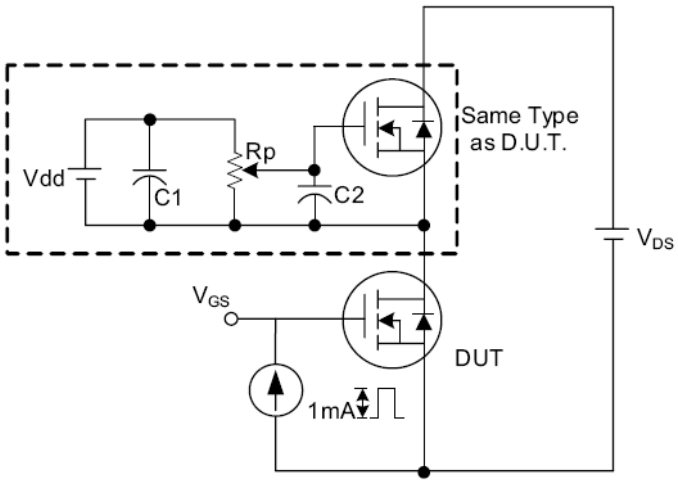


Fig. 3 . 1 Gate Charge Test Circuit

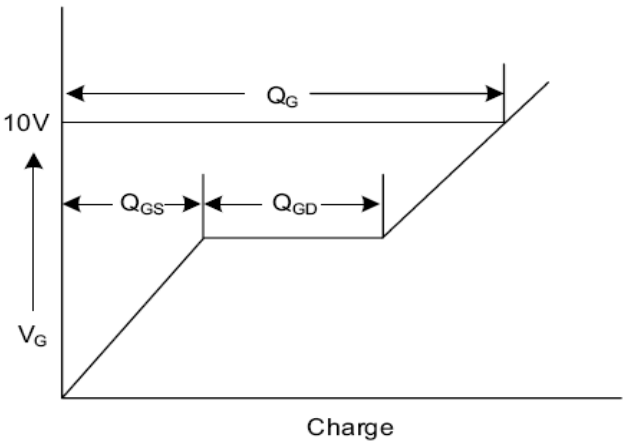


Fig. 3 . 2 Gate Charge Waveform

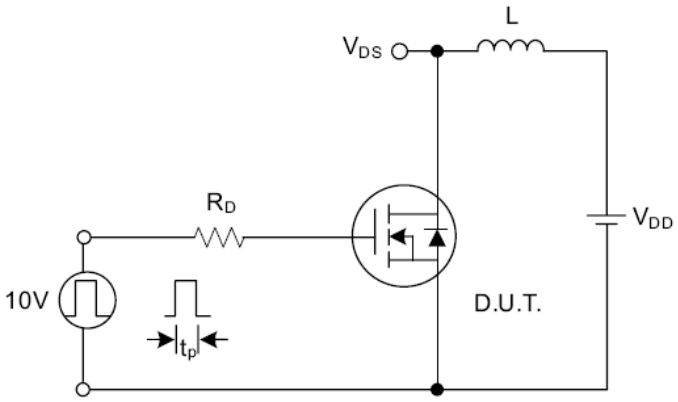


Fig. 4.1 Unclamped Inductive Switching Test Circuit

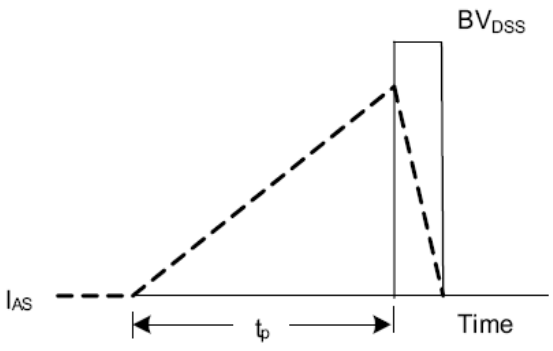
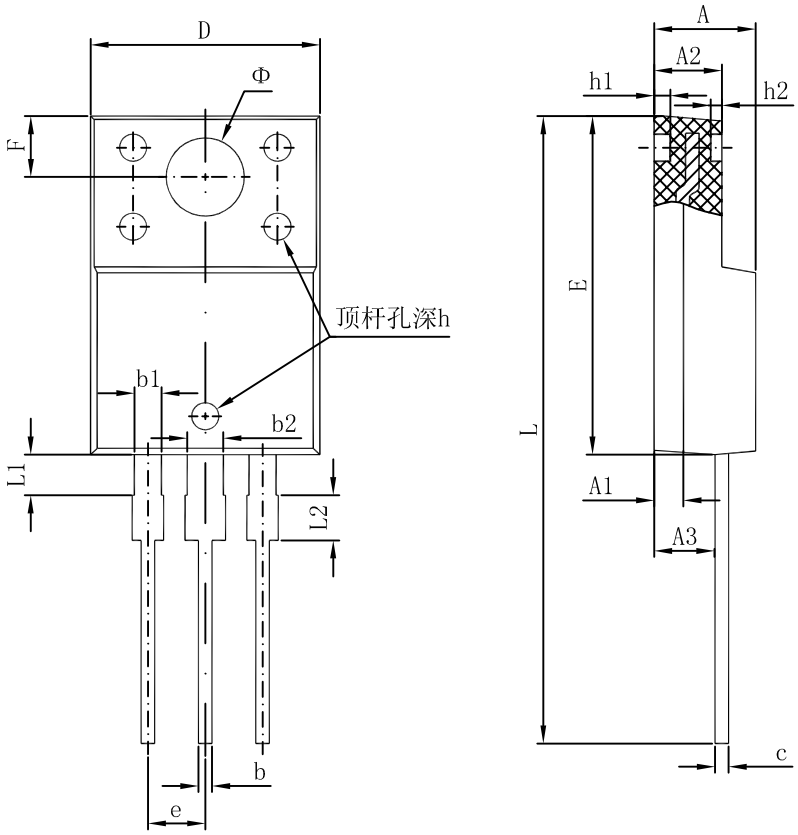


Fig. 4.2 Unclamped Inductive Switching Waveforms

Package Dimension TO-220F



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.300	4.700	0.169	0.185
A1	1.300 REF.		0.051 REF.	
A2	2.800	3.200	0.110	0.126
A3	2.500	2.900	0.098	0.114
b	0.500	0.750	0.020	0.030
b1	1.100	1.350	0.043	0.053
b2	1.500	1.750	0.059	0.069
c	0.500	0.750	0.020	0.030
D	9.960	10.360	0.392	0.408
E	14.800	15.200	0.583	0.598
e	2.540 TYP.		0.100 TYP.	
F	2.700 REF.		0.106 REF.	
Φ	3.500 REF.		0.138 REF.	
h	0.000	0.300	0.000	0.012
h1	0.800 REF.		0.031 REF.	
h2	0.500 REF.		0.020 REF.	
L	28.000	28.400	1.102	1.118
L1	1.700	1.900	0.067	0.075
L2	1.900	2.100	0.075	0.083

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