



General Description

The PSMP050N10NS2_T0_00601 use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness.

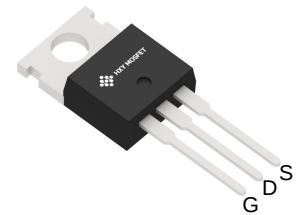
General Features

$V_{DS} = 100V$ $I_D = 120A$

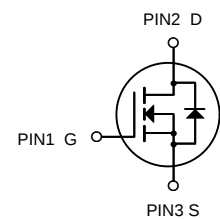
$R_{DS(ON)} < 5.0m\Omega @ V_{GS} = 10V$

Applications

Consumer electronic power supply Motor control
Synchronous-rectification Isolated DC
Synchronous-rectification applications



TO-220C



N-Channel MOSFET

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
PSMP050N10NS2_T0_00601	TO-220C	HXY MOSFET	50

Absolute Maximum Ratings at $T_J = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current $T_C = 25^\circ C$	I_D	120	A
Continuous drain current $T_C = 100^\circ C$	I_D	81	A
Pulsed drain current	I_{DM}	512	A
Power dissipation	P_D	178	W
Single pulsed avalanche energy	EAS	486	mJ
Operation and storage temperature	T_{stg}, T_J	-55 to 150	$^\circ C$
Thermal resistance, junction-case	$R_{\theta JC}$	0.8	$^\circ C/W$
Thermal resistance, junction-ambient	$R_{\theta JA}$	56	$^\circ C/W$



Electrical Characteristics($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	100	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	---	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	4.1	5.0	$m\Omega$
		$V_{GS}=4.5V$, $I_D=20A$	---	---	---	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2.0	3.0	4.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$mV/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=80V$, $V_{GS}=0V$, $T_J=100^{\circ}\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=20A$	---	35	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	1.6	---	Ω
Q_g	Total Gate Charge	$V_{DS}=50V$, $V_{GS}=10V$, $I_D=20A$	---	69	---	nC
Q_{gs}	Gate-Source Charge		---	24	---	
Q_{gd}	Gate-Drain Charge		---	18.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V$, $V_{DD}=50V$, $R_G=3\Omega$, $I_D=20A$	---	18.0	---	ns
T_r	Rise Time		---	23	---	
$T_{d(off)}$	Turn-Off Delay Time		---	37	---	
T_f	Fall Time		---	15.7	---	
C_{iss}	Input Capacitance	$V_{DS}=50V$, $V_{GS}=0V$, $f=1MHz$	---	4102	---	pF
C_{oss}	Output Capacitance		---	592	---	
C_{rss}	Reverse Transfer Capacitance		---	19.8	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	120	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3.The EAS data shows Max. rating . The test condition is $T_J = 25^{\circ}\text{C}$, $L = 3.0mH$, $I_{AS} = 18A$, $V_{GS} = 10V$, $V_{DD} = 50V$; 100% test at $L = 0.1mH$, $I_{AS} = 67A$.

4.The power dissipation is limited by 150°C junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

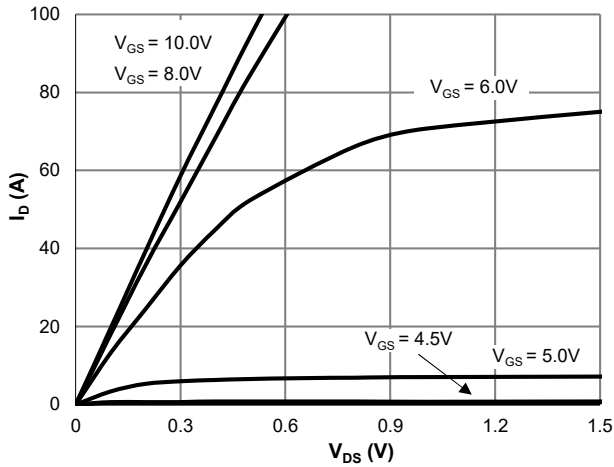


Figure 1: Saturation Characteristics

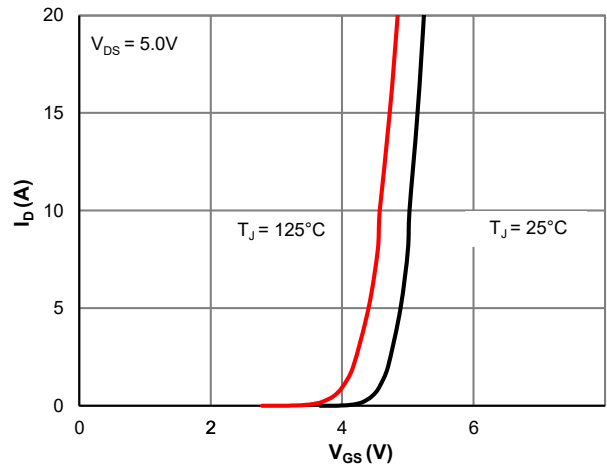


Figure 2: Transfer Characteristics

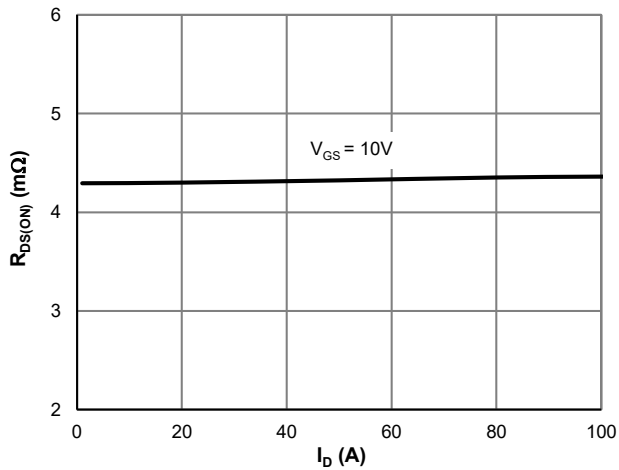


Figure 3: $R_{DS(ON)}$ vs. Drain Current

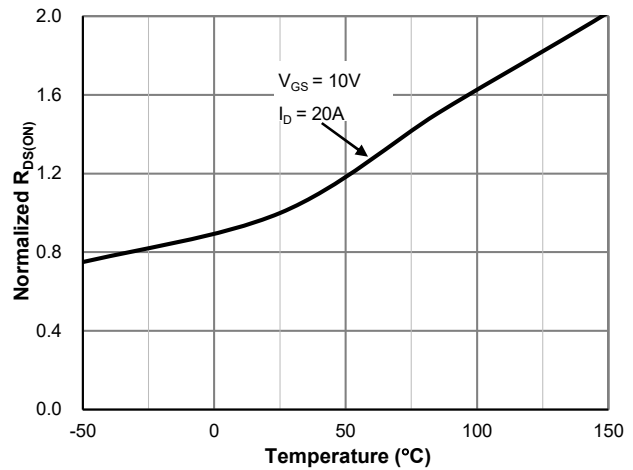


Figure 4: $R_{DS(ON)}$ vs. Junction Temperature

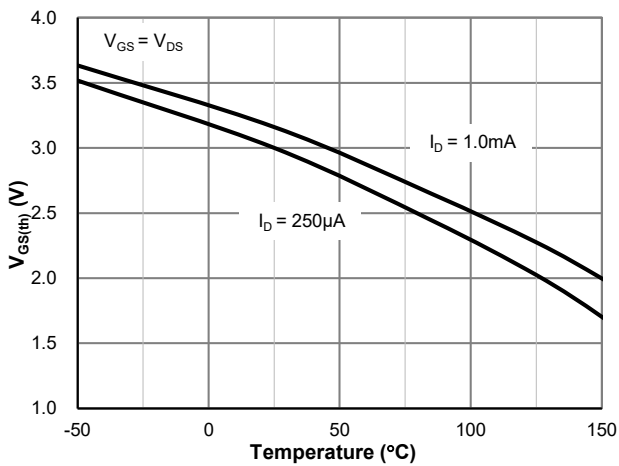


Figure 5: $V_{GS(th)}$ vs. Junction Temperature

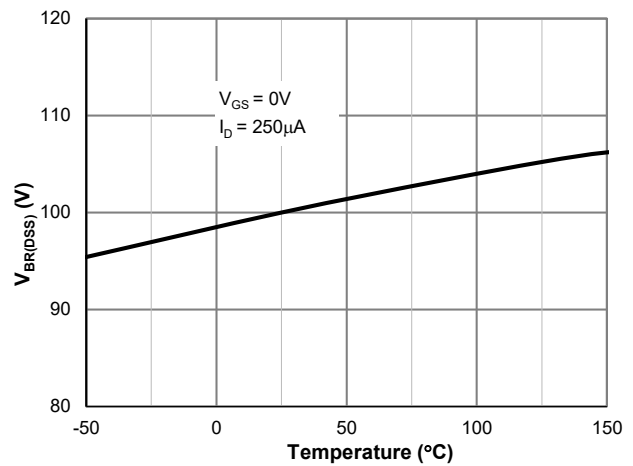


Figure 6: $V_{BR(DSS)}$ vs. Junction Temperature

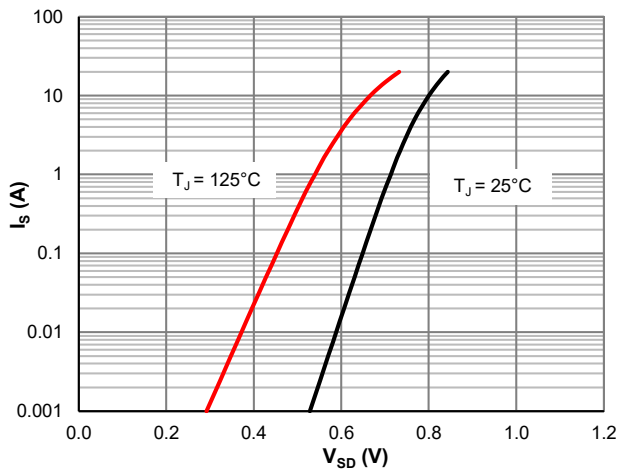


Figure 7: Body-Diode Characteristics

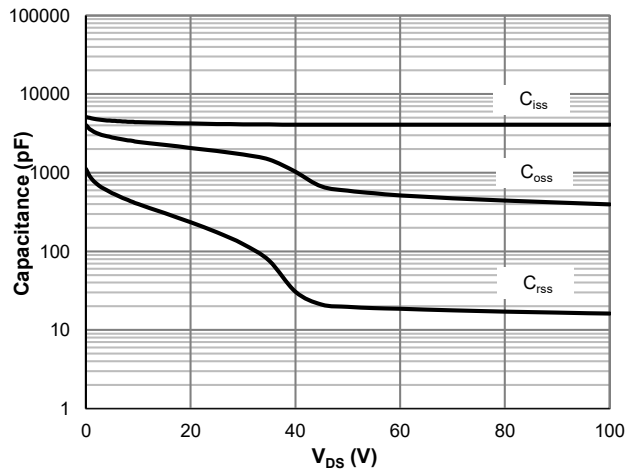


Figure 8: Capacitance Characteristics

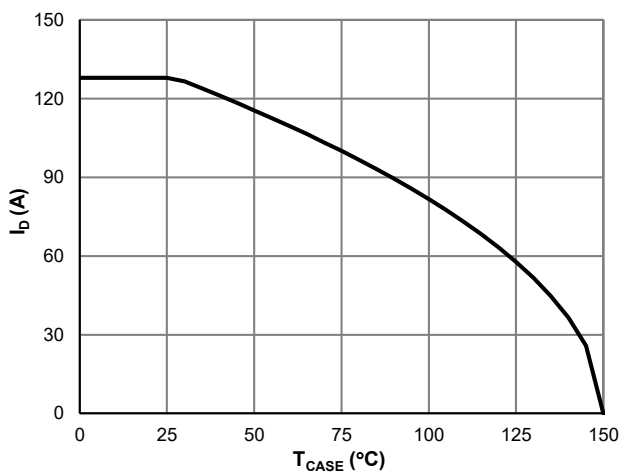


Figure 9: Current De-rating

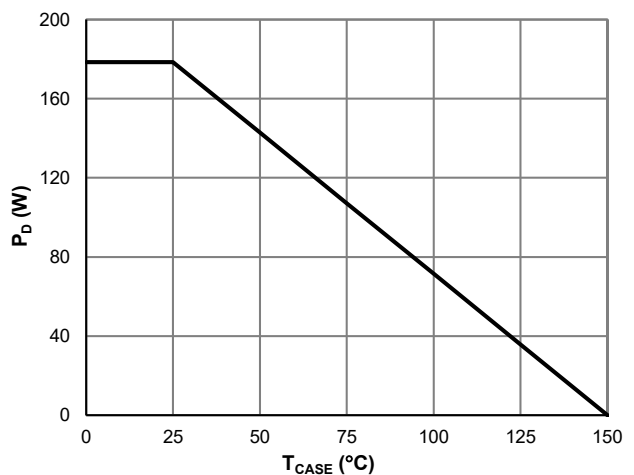


Figure 10: Power De-rating

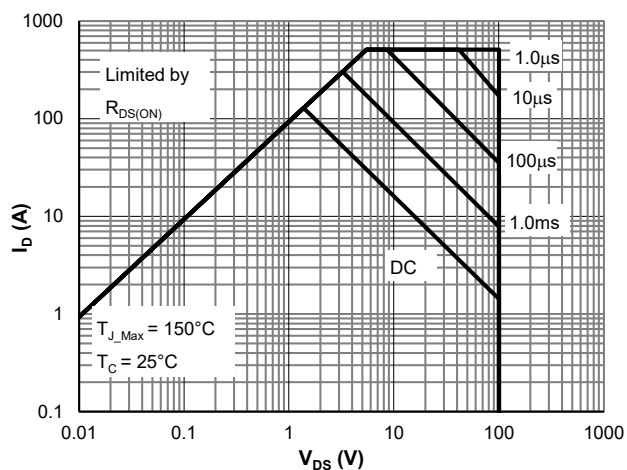


Figure 11: Maximum Safe Operating Area

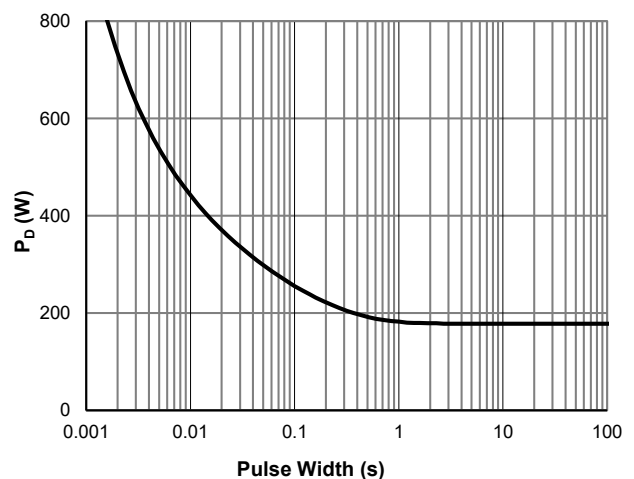


Figure 12: Single Pulse Power Rating, Junction-to-Case

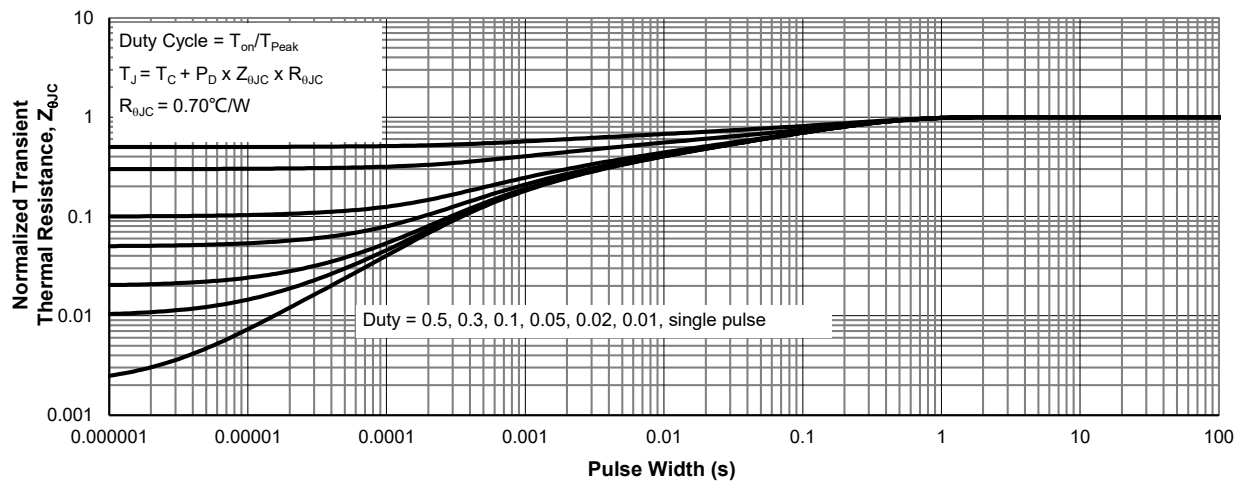
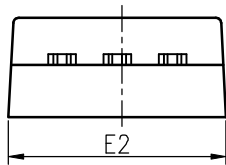
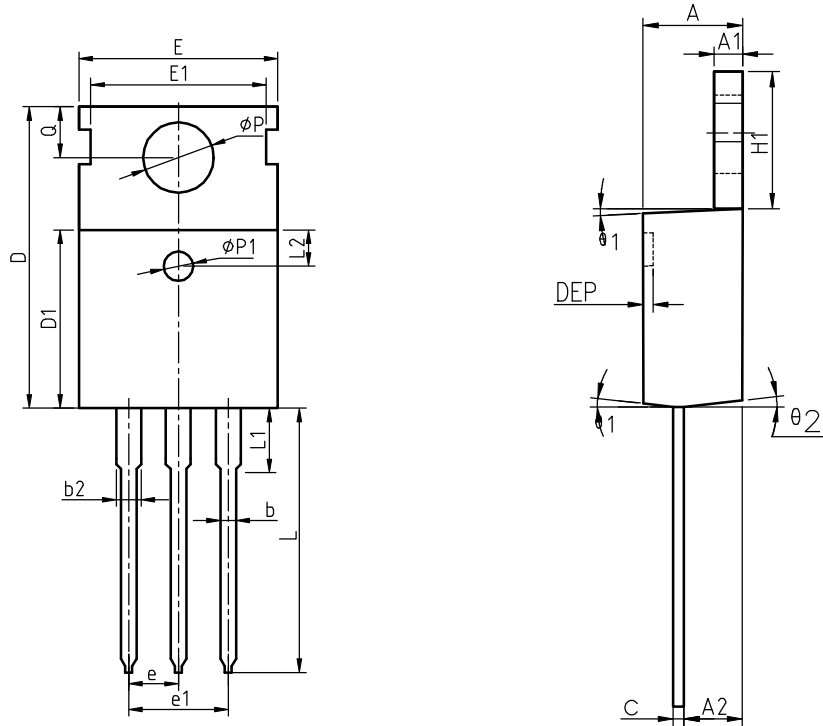


Figure 13: Normalized Maximum Transient Thermal Impedance



Package Information

TO-220C



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
θ 1	5°	7°	9°	5°	7°	9°
θ 2	1°	3°	5°	1°	3°	5°
θ 3	1°	3°	5°	1°	3°	5°



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