

Description

The DMP510DL-7 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

 $V_{DS} = -50V, I_{D} = -0.1A$

 $R_{DS(ON)}$ <5 Ω @ V_{GS} =-10V

 $R_{DS(ON)}$ <6 Ω @ V_{GS} =-4.5V

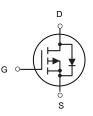
Application

Power switching application

Hard switched and high frequency circuits

DC-DC converter





P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
DMP510DL-7	SOT-23	PD	3000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	-50	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	-0.1	А
Pulsed Drain Current	I _{DM}	-0.5	А
Maximum Power Dissipation	P _D	0.35	W
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 150	°C
Thermal Resistance ,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	°C/W



Electrical Characteristics (Ta=25℃ unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Тур	Max	Unit	
Static							
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} =0, I _D =250μA	_{GS} =0, I _D =250μA -50			V	
$V_{GS(th)}$	Gate threshold voltage	V _{DS} =V _{GS} , I _D =-250μA	V _{DS} =V _{GS} , I _D =-250μA -0.8		-2.0	V	
I _{GSS}	Gate-body leakage current	V _{DS} =0, V _{GS} =±10V	V _{DS} =0, V _{GS} =±10V		±10	μA	
1	Zero gate voltage drain current	V _{DS} =-50V, V _{GS} =0V			-10	μA	
I _{DSS}		V _{DS} =-40V, V _{GS} =0V			-100	nA	
R _{DS(on)}	Drain-source on-resistance ^a	V _{GS} =-10V, I _D =-0.13A		2	5	Ω	
		V _{GS} =-4.5V, I _D =-0.13A		2.5	6	Ω	
g FS	Forward transconductance ^a	V _{DS} =-25V, I _D =-0.13A	50			mS	
V_{SD}	Diode forward voltage	I _S =-0.13A,V _{GS} =0V			-1.0	V	
Dynamic							
Ciss	Input capacitance			25			
Coss	Output capacitance	V _{DS} =-25V, V _{GS} =0V, f=1MHz		15		pF	
Crss	Reverse transfer capacitance ^b			3.5			
Switching	jb			•			
t _{d(on)}	Turn-on delay time			16.7			
t _r	Rise time	V _{GS} =-10V,V _{DS} =-15V		8.6			
$t_{d(off)}$	Turn-off delay time	I_D =-200mA, R_{GEN} =25 Ω		17.9		nS	
t _f	Fall time			5.3			

Notes:

a. Pulse Test : Pulse width≤300µs, duty cycle ≤2%. b. Guaranteed by design, not subject to producting.



Typical Characteristics

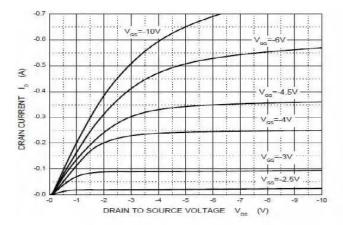


Figure 1. Output Characteristics

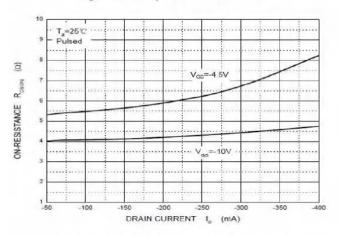


Figure3. Drain-Source on Resistance

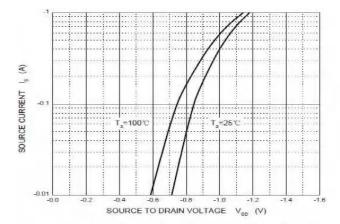


Figure 5. Diode Forward Voltage vs. current

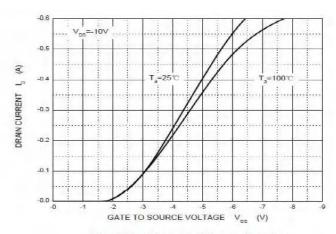


Figure 2. Transfer Characteristics

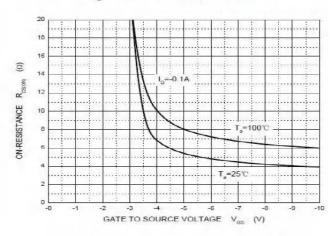


Figure 4. Drain-Source on Resistance

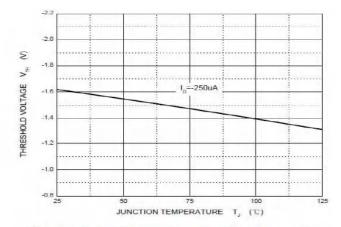
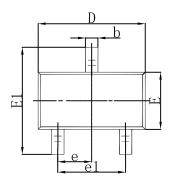
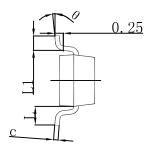


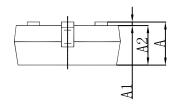
Figure 6. Gate Threshold vs. Junction Temperature



SOT-23 Package Outline Dimensions

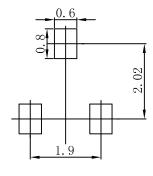






Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
Α	0.900	1.150	0.035	0.045	
A1	0.000	0.100	0.000	0.004	
A2	0.900	1.050	0.035	0.041	
b	0.300	0.500	0.012	0.020	
С	0.080	0.150	0.003	0.006	
D	2.800	3.000	0.110	0.118	
E	1.200	1.400	0.047	0.055	
E1	2.250	2.550	0.089	0.100	
е	0.950 TYP		0.037 TYP		
e1	1.800	2.000	0.071	0.079	
L	0.550 REF		0.022 REF		
L1	0.300	0.500	0.012	0.020	
θ	0°	8°	0°	8°	

SOT-23 Suggested Pad Layout



Note:

- 1. Controlling dimension: in millimeters.
- 2.General tolerance:± 0.05mm.
 3.The pad layout is for reference purposes only.

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