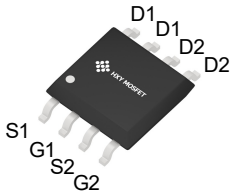
Description

The SI4932DY-T1-GE3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



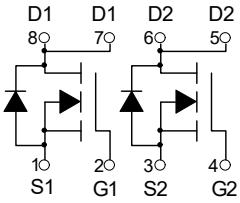
SOP-8

General Features

V_{DS} = 30V I_D = 10A

$R_{DS(ON)}$ < 12mΩ @ V_{GS}=10 V

$R_{DS(ON)}$ < 18mΩ @ V_{GS}=4.5V



Dual N-Channel MOSFET

Application

Battery protection

Load switch

Uninterruptible power supply

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
SI4932DY-T1-GE3	SOP-8	HXY MOSFET	3000

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Drain Current, V_{GS} @ 4.5V[3]	10	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 4.5V[3]	8	A
I_{DM}	Pulsed Drain Current[1]	55	A
P_D@T_A=25℃	Total Power Dissipation	2	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

Electrical Characteristics Ta = 25°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	uA
		V_{DS}=30V, V_{GS}=0V, T_J=55℃			5	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=250uA	1.5		2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A			12	mΩ
		V_{GS}=10V, I_D=10A T_J=125℃			18	
		V_{GS}=4.5V, I_D=8A			16.5	
On State Drain Current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	55			A
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=10A		43		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	610		910	pF
Output Capacitance	C_{oss}		88		160	
Reverse Transfer Capacitance	C_{rss}		40		100	
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.8		2.4	Ω
Total Gate Charge (10V)	Q_g	V_{GS}=10V, V_{DS}=15V, I_D=10A	11		17	nC
Total Gate Charge (4.5V)			5		8	
Gate Source Charge	Q_{gs}			2.4		
Gate Drain Charge	Q_{gd}			3		
Turn-On DelayTime	$t_{d(on)}$	V_{GS}=10V, V_{DS}=15V, R_L=1.5Ω, R_{GEN}=3Ω		4.4		ns
Turn-On Rise Time	t_r			9		
Turn-Off DelayTime	$t_{d(off)}$			17		
Turn-Off Fall Time	t_f			6		
Body Diode Reverse Recovery Time	t_{rr}	I_F= 10A, dI/dt= 500A/us	5.6		8	
Body Diode Reverse Recovery Charge	Q_{rr}		6.4		9.6	nC
Maximum Body-Diode Continuous Current	I_S				2.5	A
Diode Forward Voltage	V_{SD}	I_S=1A,V_{GS}=0V			1	V

Note.The static characteristics in Figures 1 to 6 are obtained using <300us pulses, duty cycle 0.5% max.

Typical Characterisitics

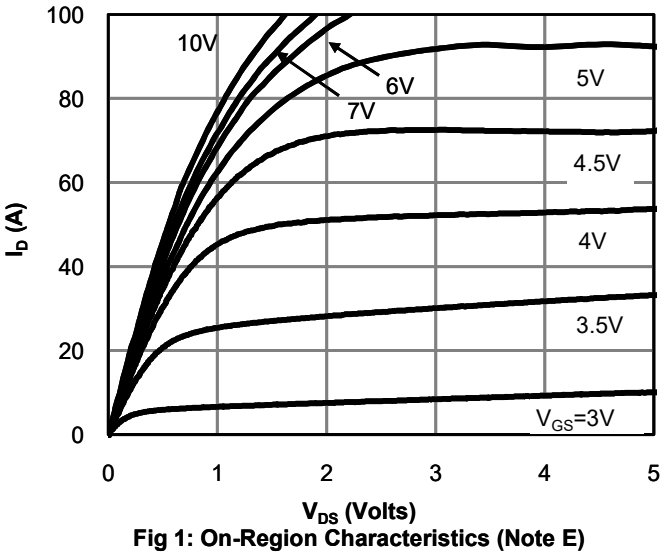


Fig 1: On-Region Characteristics (Note E)

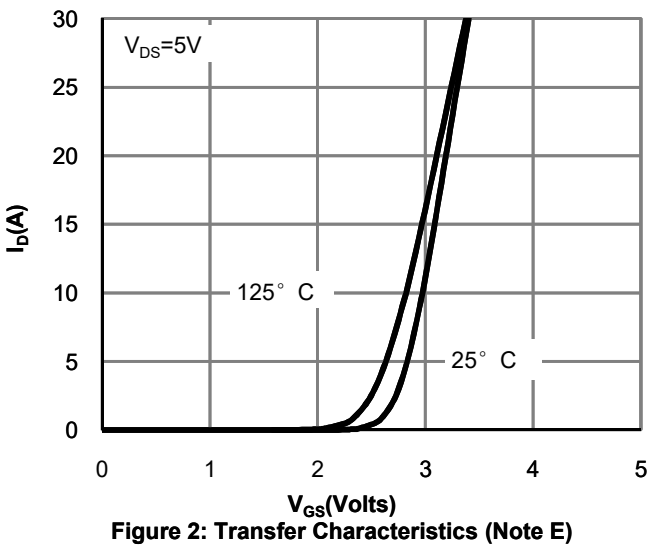


Figure 2: Transfer Characteristics (Note E)

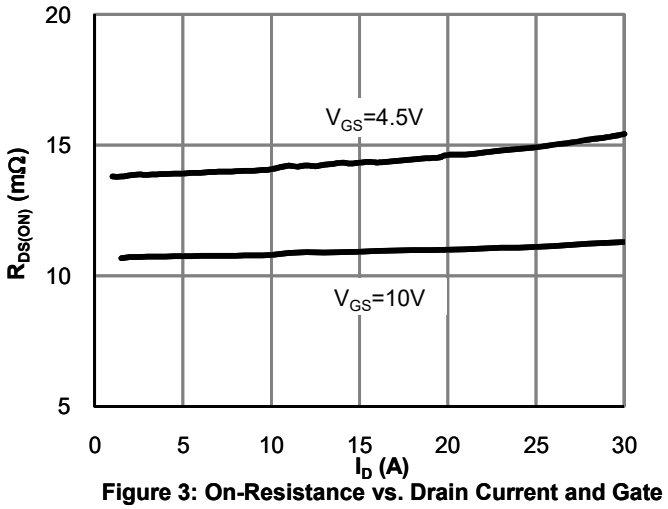


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

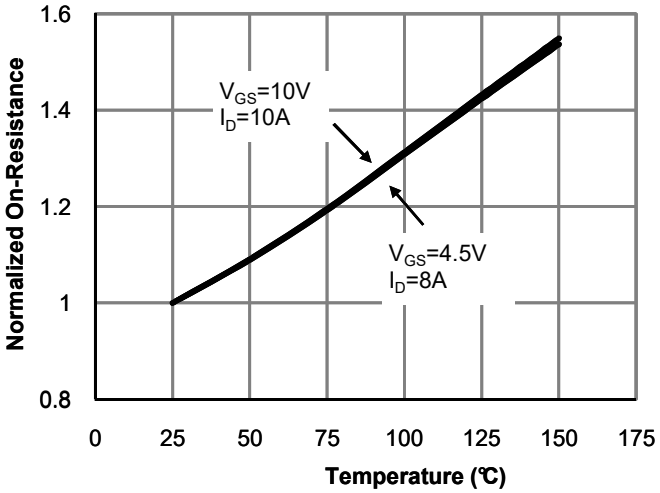


Figure 4: On-Resistance vs. Junction Temperature (Note E)

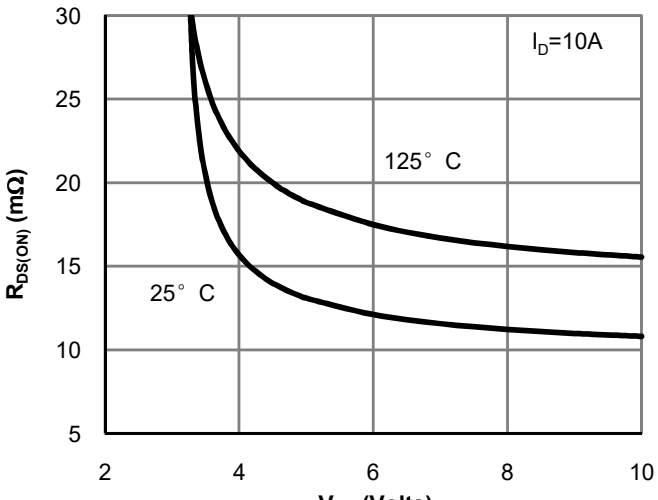


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

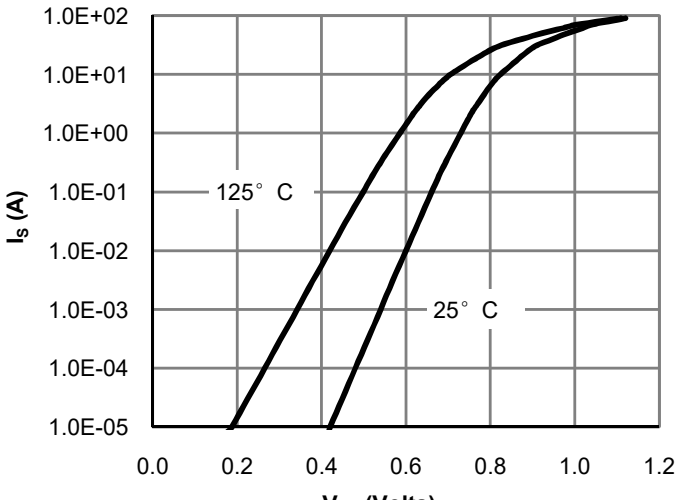


Figure 6: Body-Diode Characteristics (Note E)

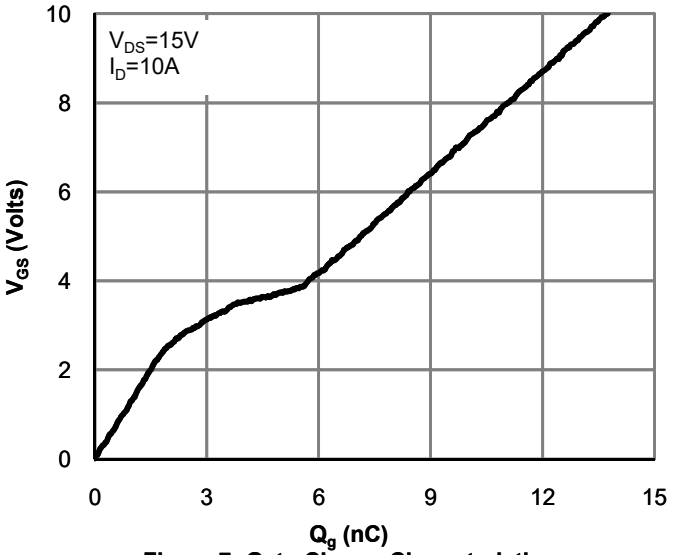


Figure 7: Gate-Charge Characteristics

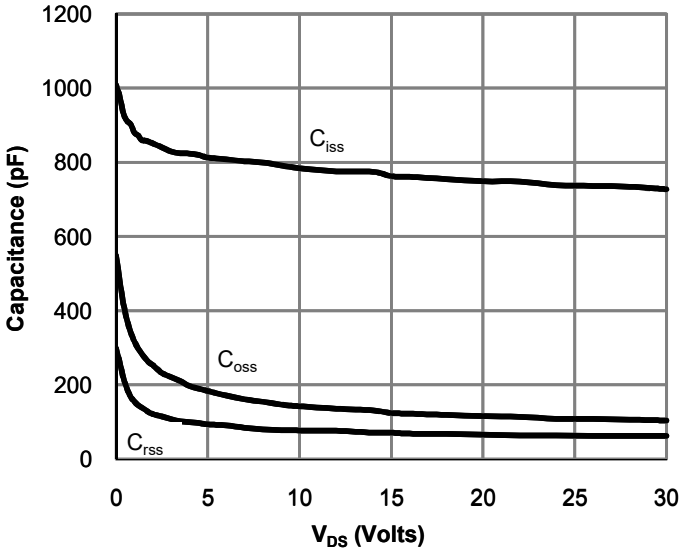


Figure 8: Capacitance Characteristics

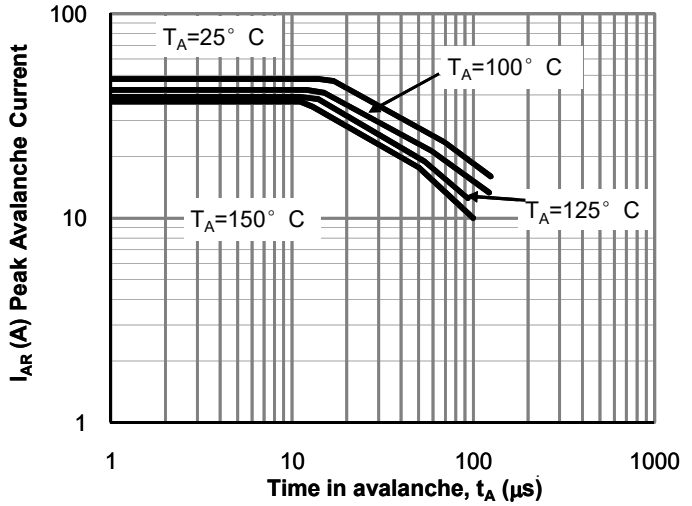


Figure 9: Single Pulse Avalanche capability (Note C)

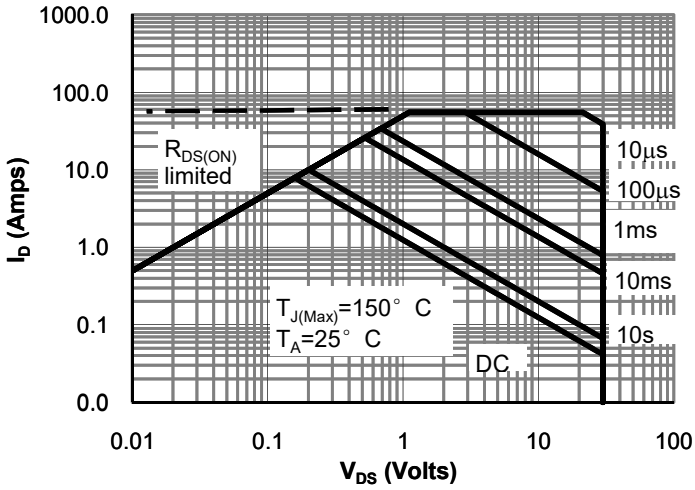


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

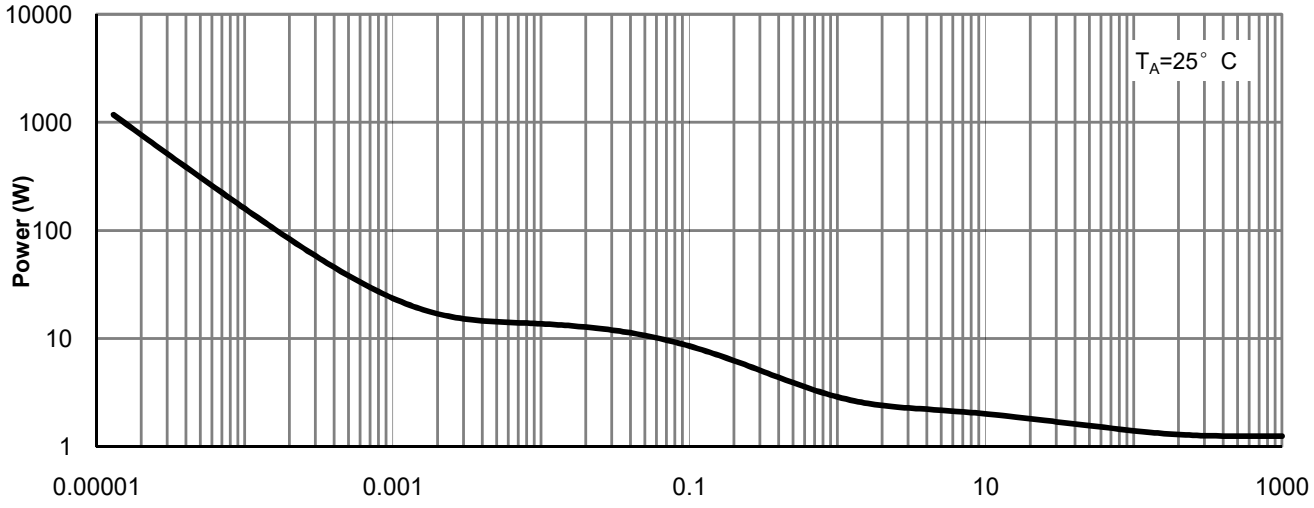


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

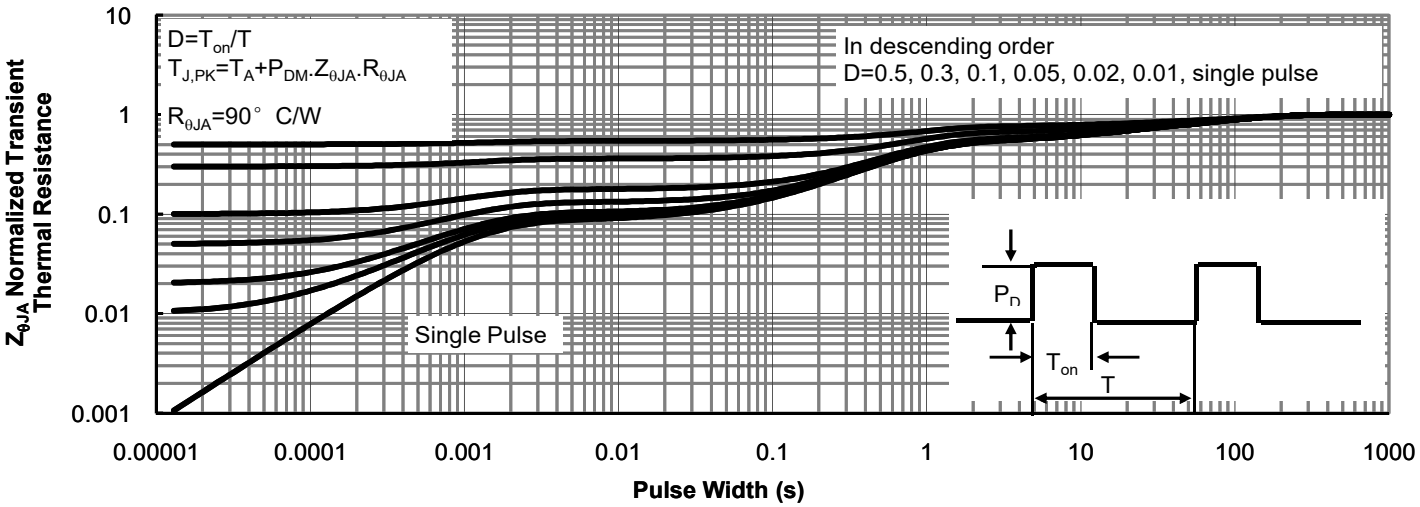
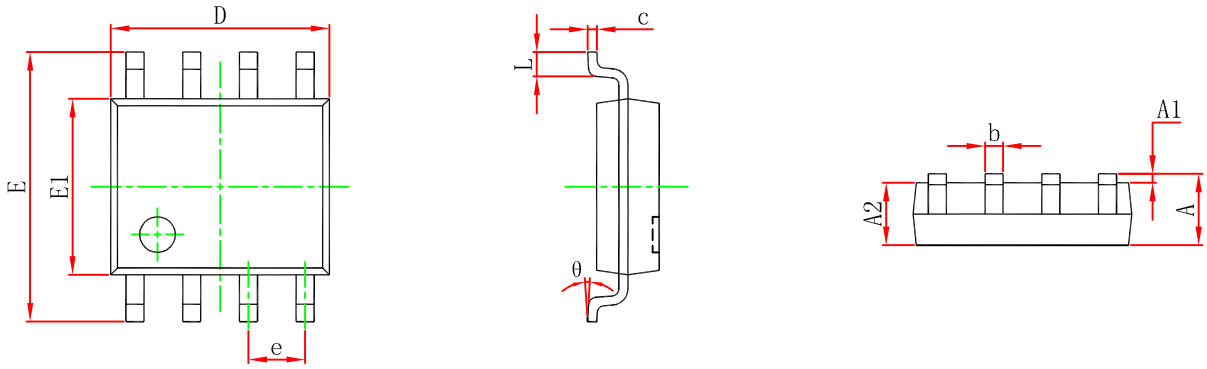
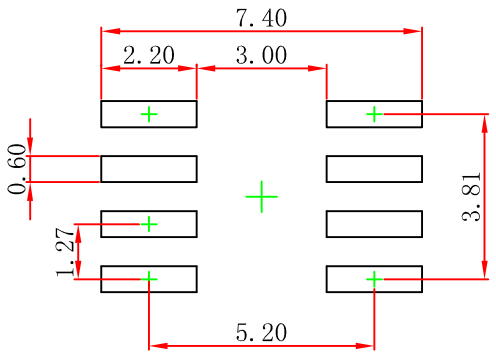


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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