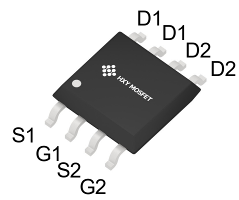
Description

The DMC3025LSD-13 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8
(SOIC-8)

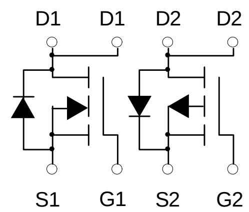
General Features

V_{DS} = 30V I_D =6A

$R_{DS(ON)}$ < 22mΩ @ V_{GS}=10V

V_{DS} = -30V I_D =-5.5A

$R_{DS(ON)}$ < 45 mΩ @ V_{GS}=-10V



N-Channel and P-Channel

Application

Wireless charging

Boost driver

Brushless motor

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
DMC3025LSD-13	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings (T_C=25°C unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
VDS	Drain-Source Voltage	30	-30	V
VGS	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	6	-5.5	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	5	-4.3	A
IDM	Pulsed Drain Current[2]	30	-30	A
EAS	Single Pulse Avalanche Energy[3]	5	26	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	2	2	W
TSTG	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	62.5		℃/W
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	40		℃/W

N-Channel Electrical Characteristics (T_J =25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.2	1.8	2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=6A		16	22	mΩ
		T_J=125℃		32	40	
		V_{GS}=4.5V, I_D=5A		22	30	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6A		15		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
Dynamic Parameters						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	200	255	310	pF
C_{oss}	Output Capacitance		30	45	60	pF
C_{rss}	Reverse Transfer Capacitance		20	35	50	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.6	3.25	4.9	Ω
Switching Parameters						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=6A	4	5.2	6	nC
Q_g(4.5V)	Total Gate Charge		2	2.55	3	nC
Q_{gs}	Gate Source Charge			0.85		nC
Q_{gd}	Gate Drain Charge			1.3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2.5Ω, R_{GEN}=3Ω		4.5		ns
t_r	Turn-On Rise Time			2.5		ns
$t_{D(off)}$	Turn-Off DelayTime			14.5		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=6A, dI/dt=100A/µs		8.5	12	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=6A, dI/dt=100A/µs		2.2	3	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ⩽ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

Typical Characteristics

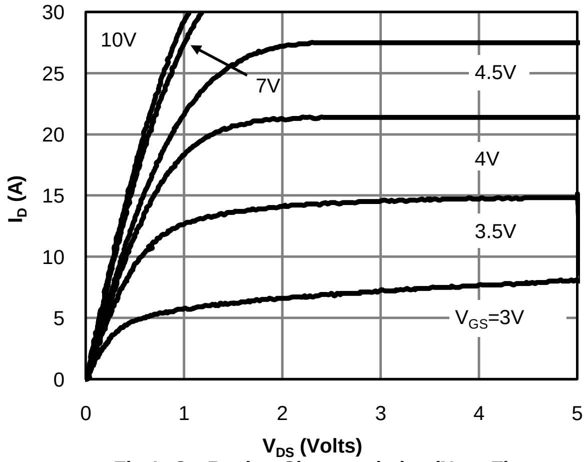


Fig 1: On-Region Characteristics (Note E)

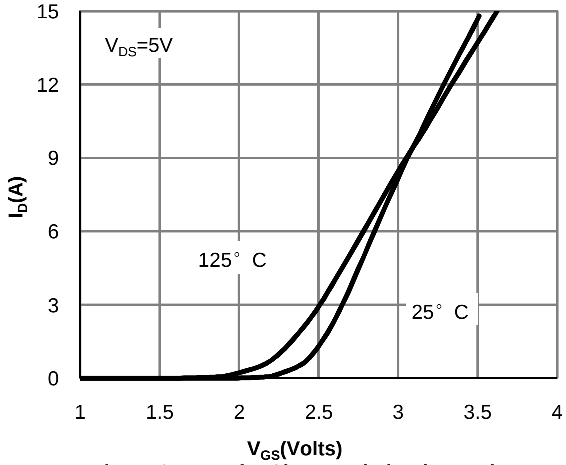


Figure 2: Transfer Characteristics (Note E)

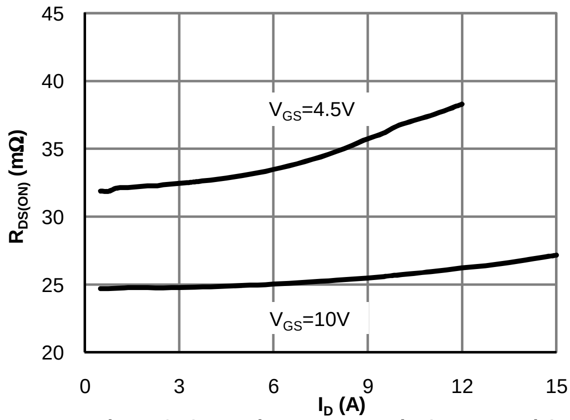


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

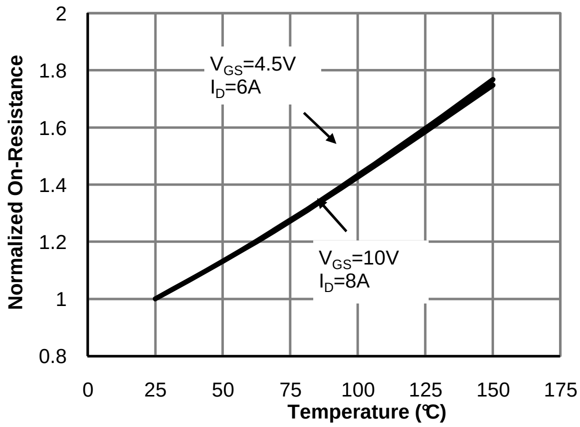


Figure 4: On-Resistance vs. Junction Temperature (Note E)

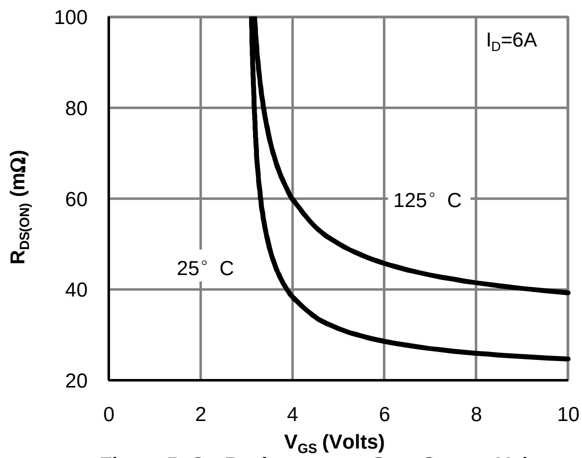


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

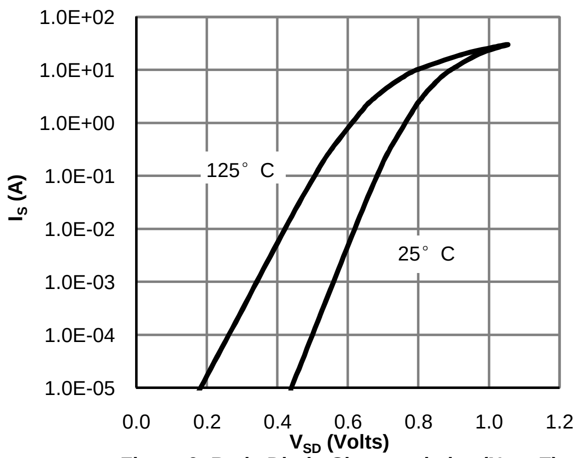


Figure 6: Body-Diode Characteristics (Note E)

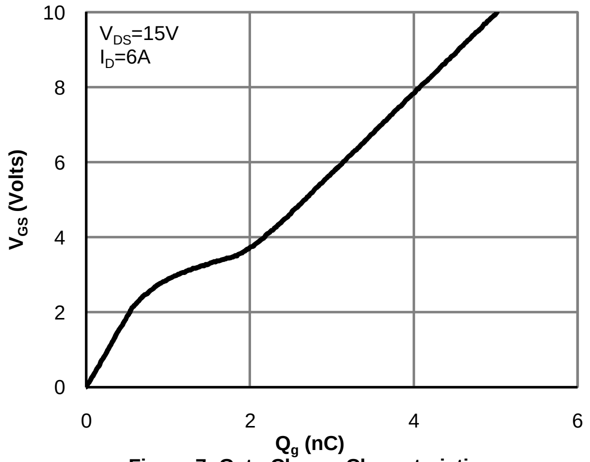


Figure 7: Gate-Charge Characteristics

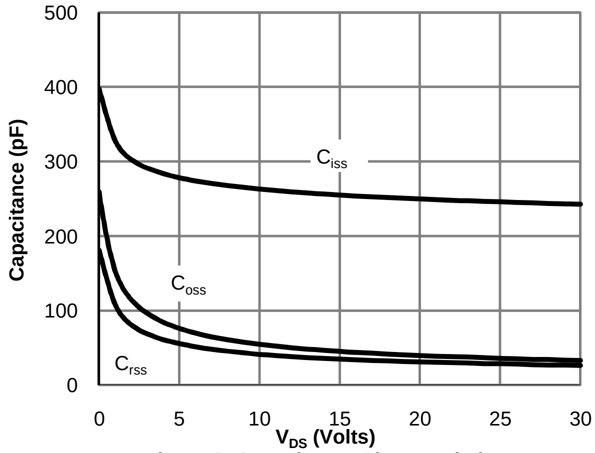


Figure 8: Capacitance Characteristics

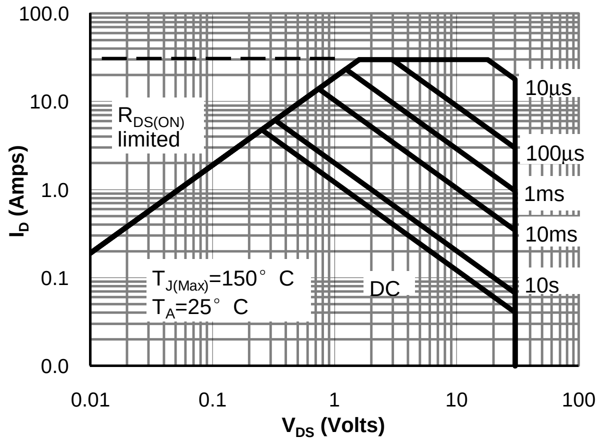


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

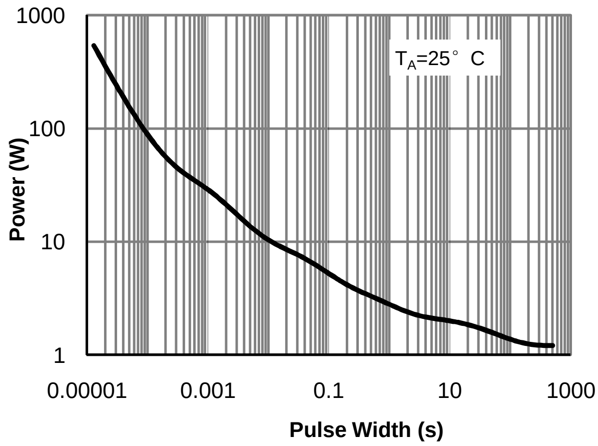


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

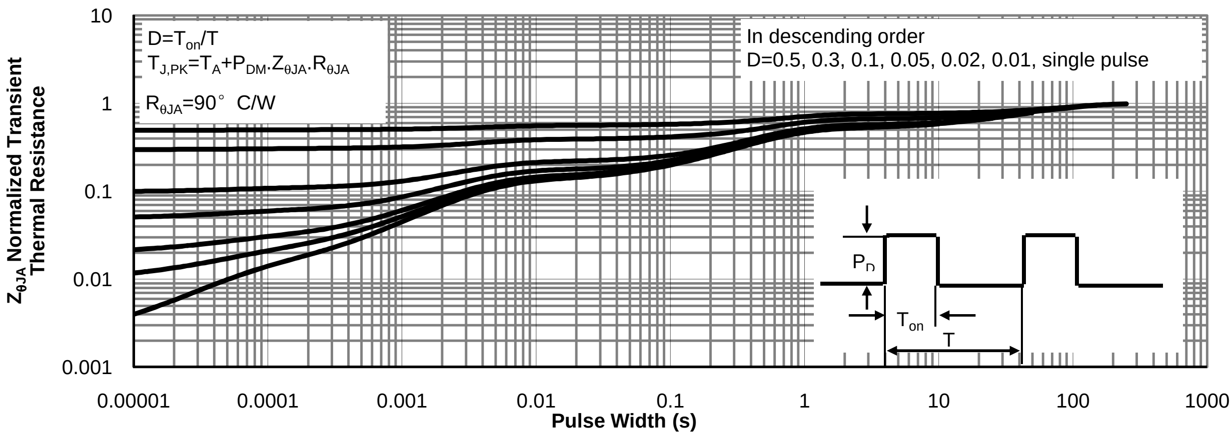
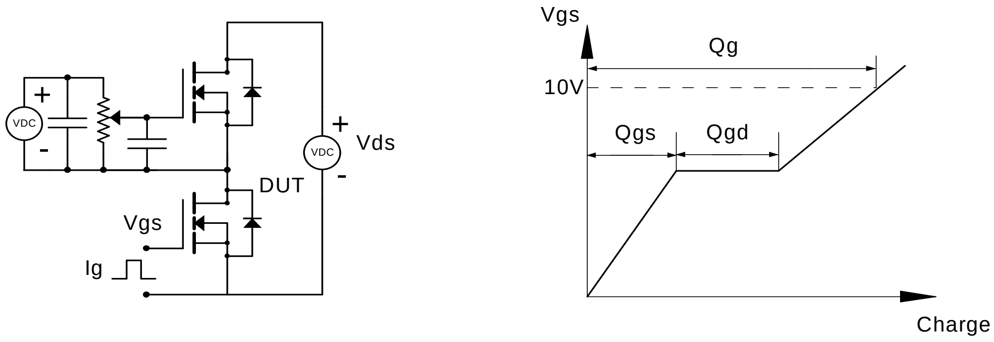
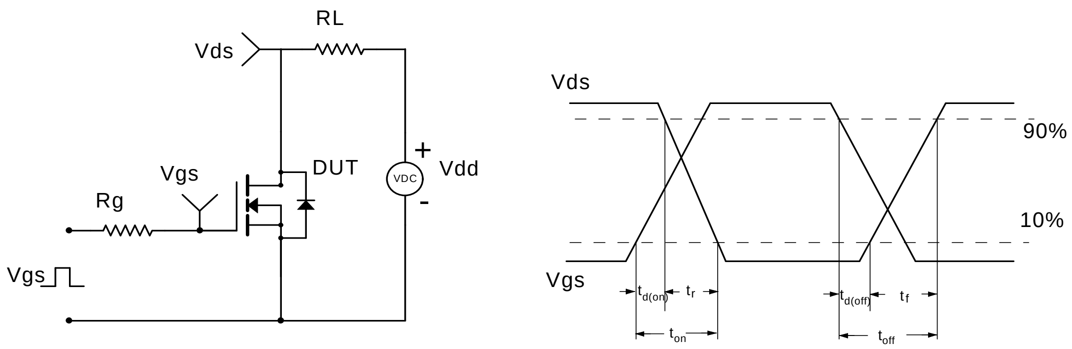


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

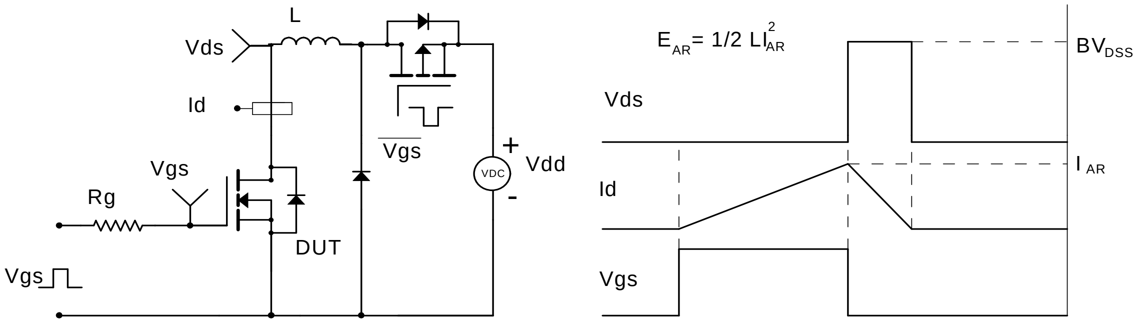
Gate Charge Test Circuit & Waveform



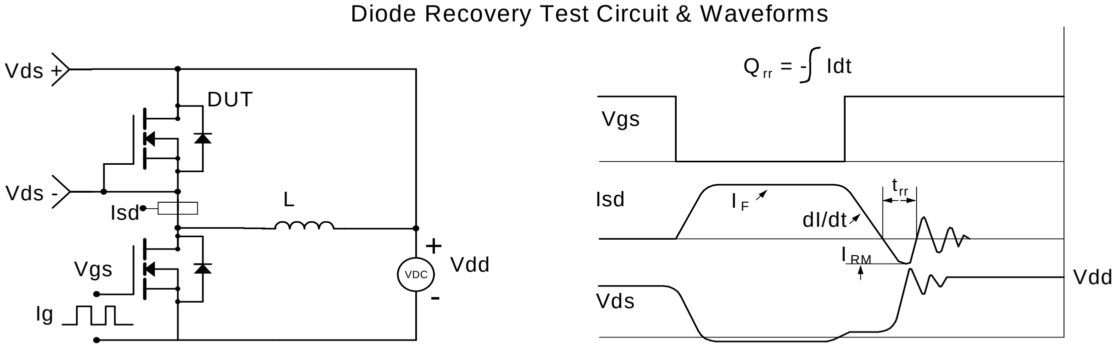
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J =25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static Parameters						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250µA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	µA
		T_J=55℃			-5	µA
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-1.3	-1.85	-2.4	V
$I_{D(ON)}$	On state drain current	V_{GS}=-10V, V_{DS}=-5V	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-6.5A		36	45	mΩ
		T_J=125℃		32	40	mΩ
		V_{GS}=-4.5V, I_D=-5A		68	77	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-6.5A		18		S
V_{SD}	Diode Forward Voltage	I_S=-1A,V_{GS}=0V		-0.8	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.5	A
Dynamic Parameters						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz		760		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			95		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.5	3.2	5	Ω
Switching Parameters						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=-15V, I_D=-6.5A		13.6	16	nC
Q_g(4.5V)	Total Gate Charge			6.7	8	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3.2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=-15V, R_L=2.3Ω, R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-6.5A, dI/dt=100A/µs		15		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-6.5A, dI/dt=100A/µs		9.7		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

Typical Characteristics

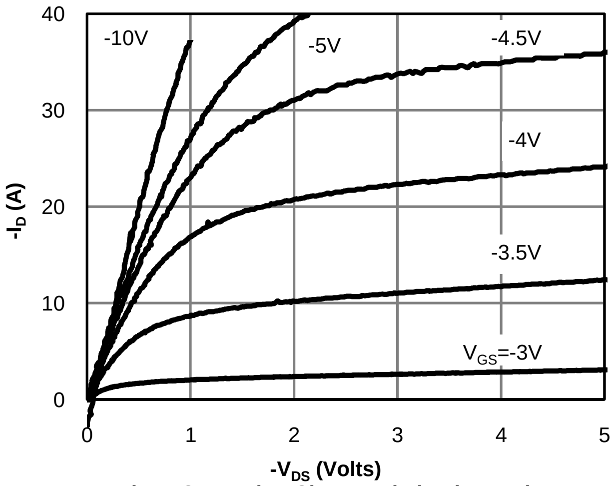


Fig 1: On-Region Characteristics (Note E)

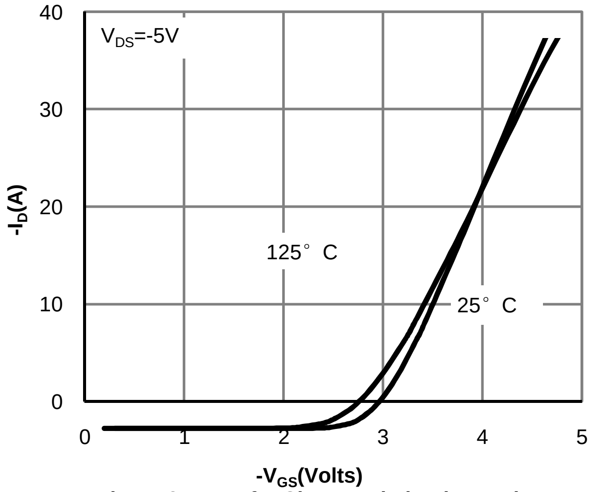


Figure 2: Transfer Characteristics (Note E)

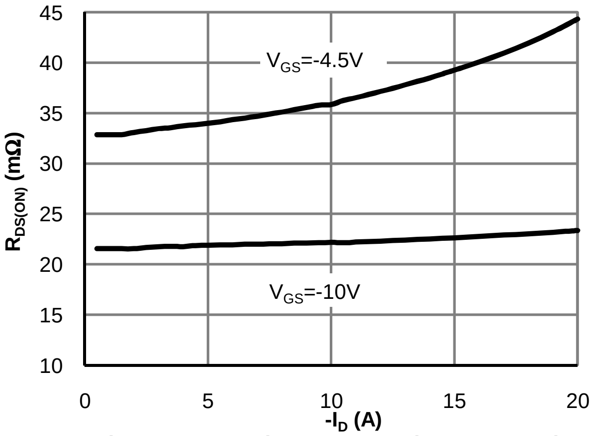


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

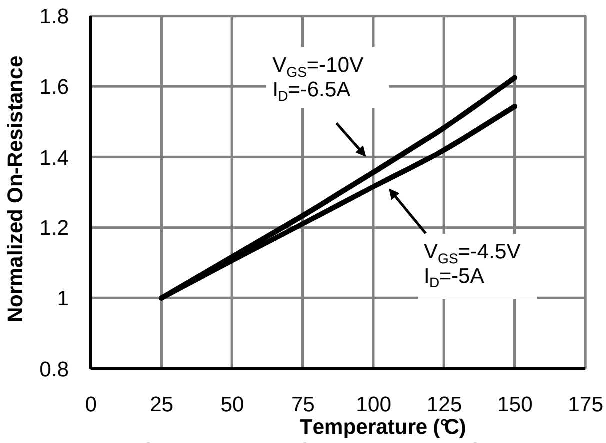


Figure 4: On-Resistance vs. Junction Temperature (Note E)

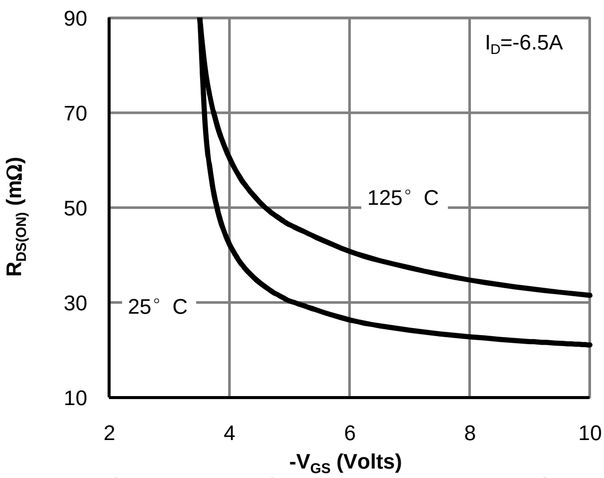


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

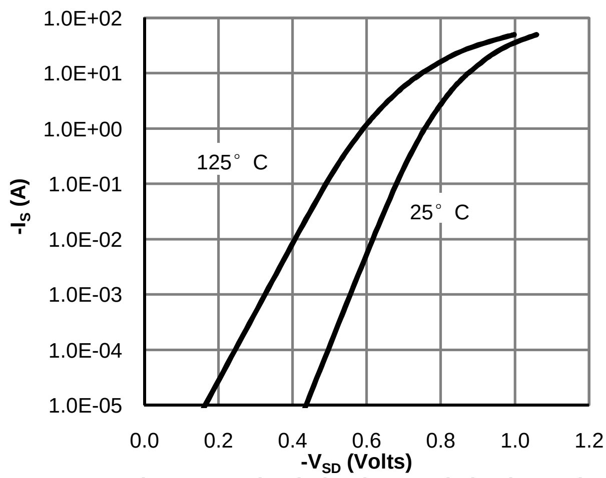


Figure 6: Body-Diode Characteristics (Note E)

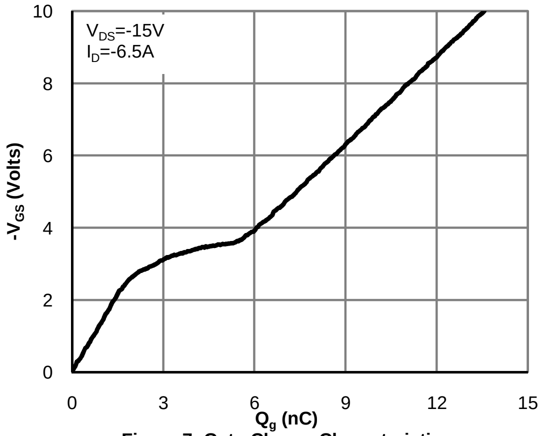


Figure 7: Gate-Charge Characteristics

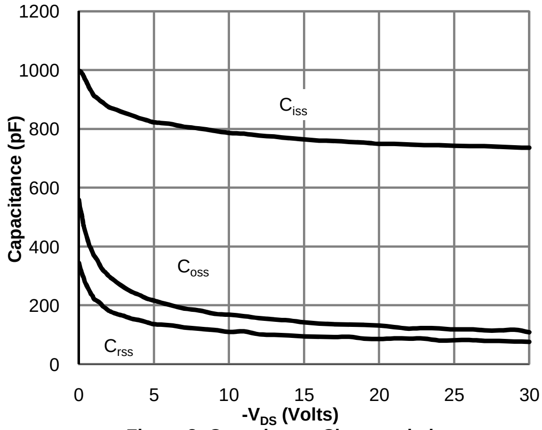


Figure 8: Capacitance Characteristics

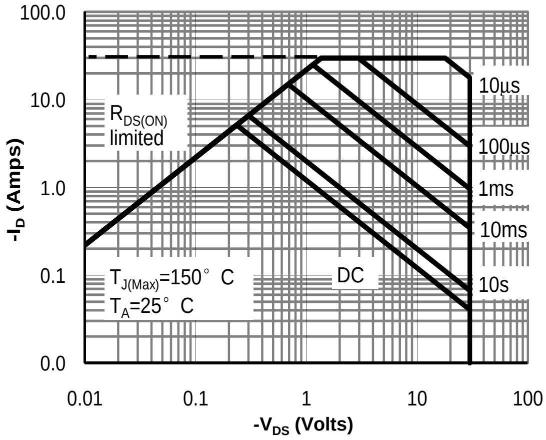


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

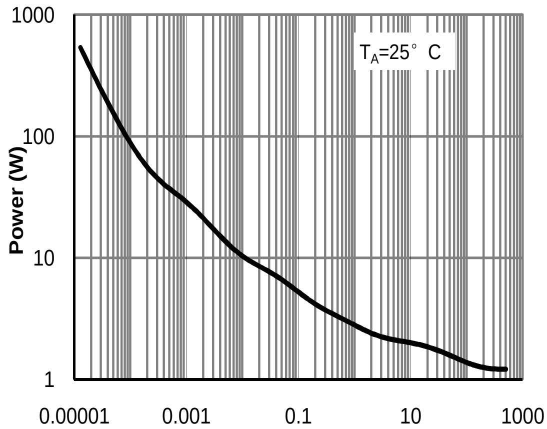


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

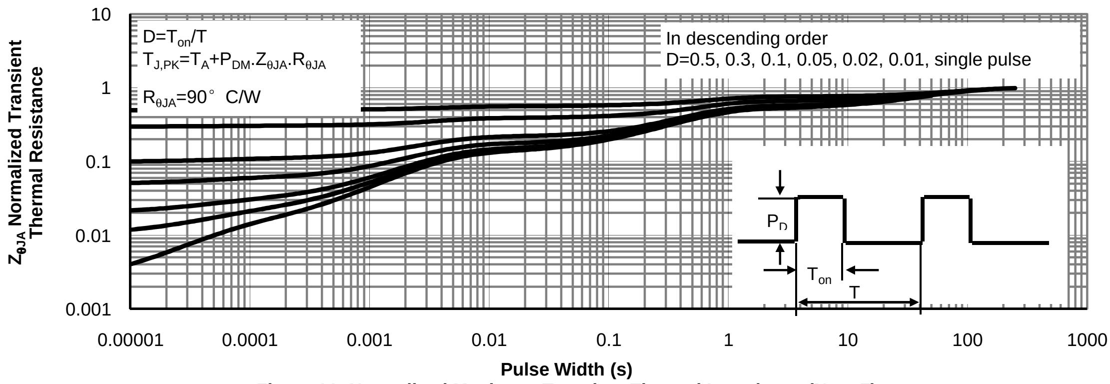
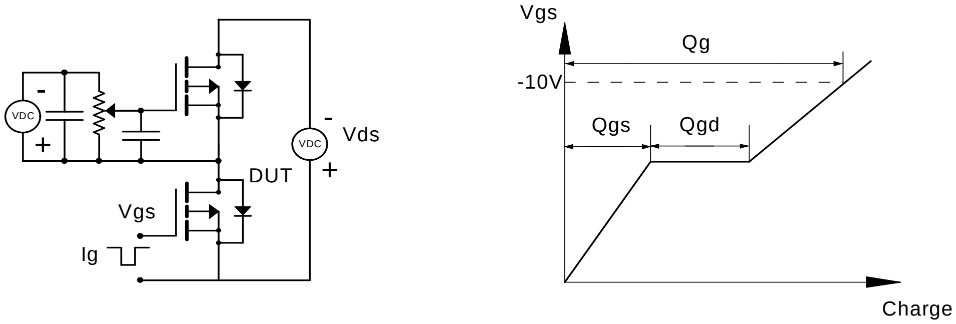
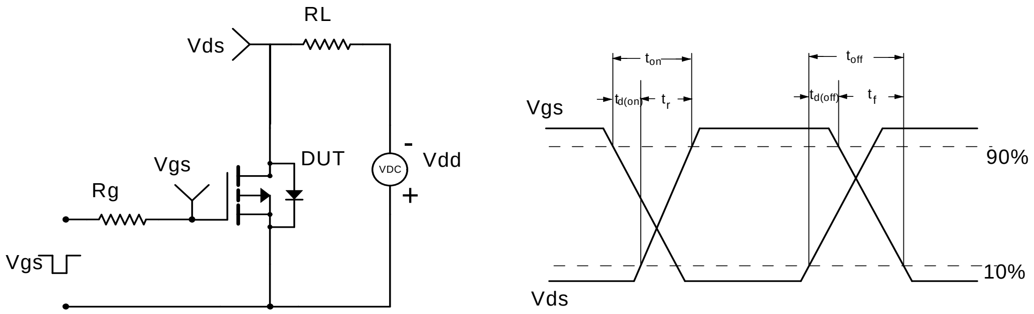


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

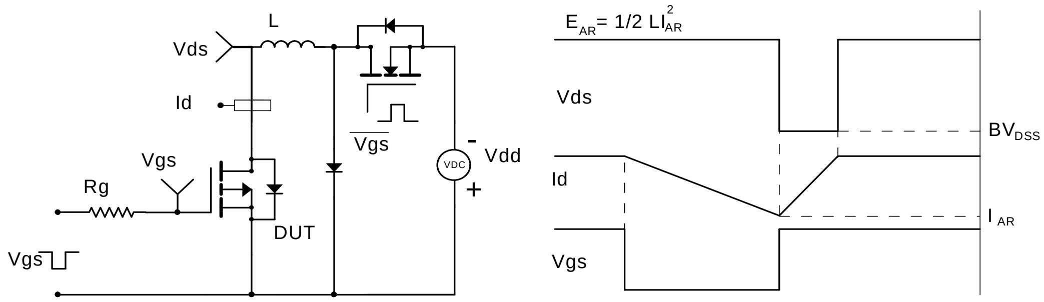
Gate Charge Test Circuit & Waveform



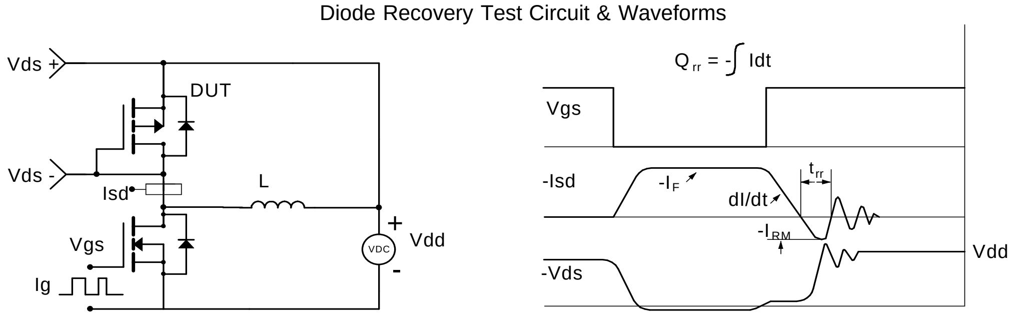
Resistive Switching Test Circuit & Waveforms



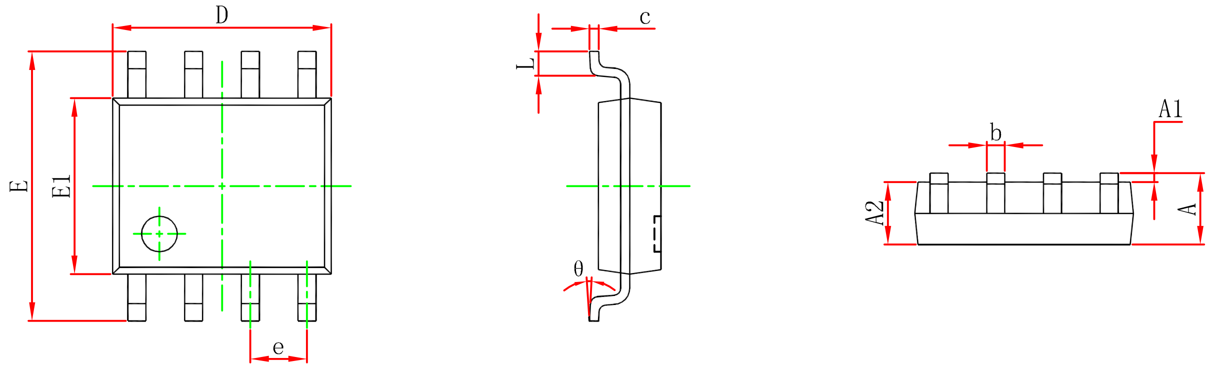
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



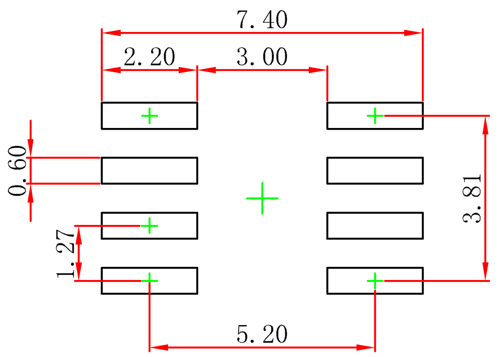
Diode Recovery Test Circuit & Waveforms



SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1. 350	1. 750	0. 053	0. 069
A1	0. 100	0. 250	0. 004	0. 010
A2	1. 350	1. 550	0. 053	0. 061
b	0. 330	0. 510	0. 013	0. 020
c	0. 170	0. 250	0. 007	0. 010
D	4. 800	5. 000	0. 189	0. 197
e	1. 270 (BSC)		0. 050 (BSC)	
E	5. 800	6. 200	0. 228	0. 244
E1	3. 800	4. 000	0. 150	0. 157
L	0. 400	1. 270	0. 016	0. 050
θ	0°	8°	0°	8°



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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