

#### **Description**

The HBSC065N06LS5 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

V<sub>DS</sub> = 60V I<sub>D</sub> =80 A

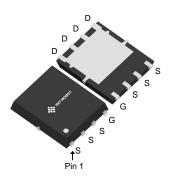
 $R_{DS(ON)} < 7m\Omega$  @  $V_{GS}=10V$ 

## **Application**

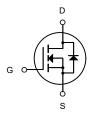
**Battery protection** 

Load switch

Uninterruptible power supply



DFN5X6-8L (TDSON-8(5.9x5.2))



N-Channel MOSFET

## **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
HBSC065N06LS5	DFN5X6-8L(TDSON-8(5.9x5.2))	HXY MOSFET	5000

### Absolute Maximum Ratings (T<sub>c</sub>=25<sup>°</sup>Cunless otherwise noted)

Symbol	Parameter Rating		Units	
Vps	Drain-Source Voltage	60	V	
Vgs	Gate-Source Voltage	±20	V	
I <sub>D</sub> @T <sub>C</sub> =25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	А		
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	А		
Ірм	Pulsed Drain Current <sup>2</sup> 320		А	
EAS	Single Pulse Avalanche Energy <sup>3</sup>	169	mJ	
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	tal Power Dissipation <sup>4</sup> 108		
Тѕтс	Storage Temperature Range	-55 to 150		
TJ	Operating Junction Temperature Range	-55 to 150	°C	
Rejc	R <sub>0</sub> JC Thermal Resistance Junction-Case <sup>1</sup>		°C/W	



# **Electrical Characteristics** (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Conditi <b>a</b>	Min.	Тур.	Max.	Units
Off Charac	cteristic				.1	I
V <sub>(BR)DS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	_	_	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V, -		-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	-	-	±100	nA
On Claract	teristics					
$V_{GS(th)}$	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =2 50μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> = 30A	-	5.3	7	mΩ
Dynamic (	Characteristics			•	-	
C <sub>iss</sub>	Input Capacita <b>e</b> c	V <sub>DS</sub> =30V,	-	4136	-	pF
$C_{oss}$	Output Capacitance	V <sub>GS</sub> =0V,	ı	286	-	pF
$C_{rss}$	Reverse Transfer Capacitance	f=1.0MHz	ı	257	-	pF
$\mathbf{Q}_{g}$	Total Gate Charge	V <sub>DS</sub> =30V,	ı	90	-	nC
$Q_gs$	Gate-Source Charge	V <sub>DS</sub> −30V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	•	9	-	nC
$Q_gd$	Gate-Drain("Miller") Charge	1D-30A, VGS-10V	-	18	-	nC
Switching	Characteristics					
t <sub>d(on)</sub>	Turn-on Delay Time		-	9	-	ns
t <sub>r</sub>	Turn-on Rise Time	V <sub>DS</sub> =30V, I <sub>D</sub> =30A,	-	7	-	ns
$t_{d(off)}$	Turn-off Delay Time	R <sub>G</sub> =1.8Ω, V <sub>GS</sub> =10V	-	40	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	15	-	ns
DrainSour	ce Diode Characteristics and Maximu	ım Ratings				
Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	80	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Dio	urce Diode Forward Current		-	320	Α
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0VI <sub>S</sub> =30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time		-	33	-	ns
Qrr	Body Diode Reverse Recovery Charge	I <sub>F</sub> =30A, dI/dt=100A/μs	-	46	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

- 2. EAS condition : T<sub>J</sub>=25  $^{\circ}$ C, V<sub>DD</sub>=30V, V<sub>G</sub>=10V, L=0.5mH, Rg=25 $\Omega$ , I<sub>AS</sub>=26A
- 3. Pulse Test: Pulse Width≤300µs, Duty Cycle≤0.5%



## **Typical Performance Characteristics**

Figure1: Output Characteristics

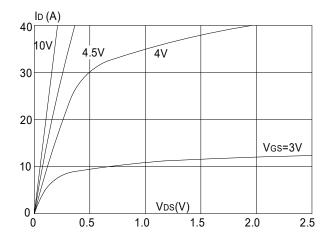


Figure 2: Typical Transfer Characteristics

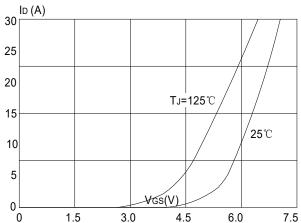


Figure 3:On-resistance vs. Drain Current

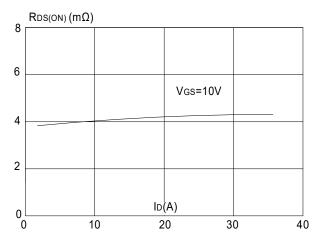


Figure 4: Body Diode Characteristics

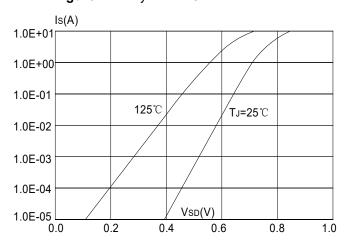


Figure 5: Gate Charge Characteristics

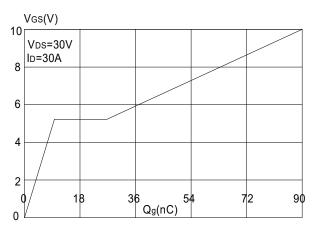
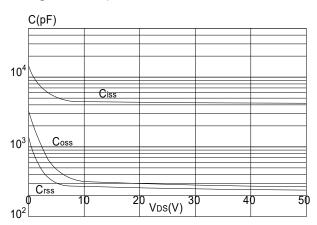


Figure 6: Capacitance Characteristics





**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature

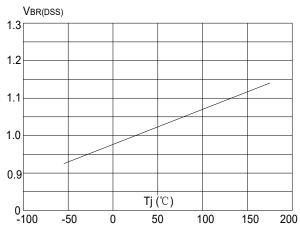
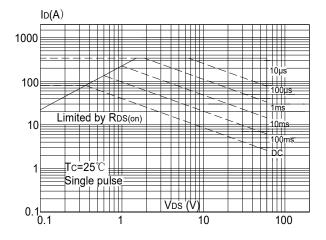
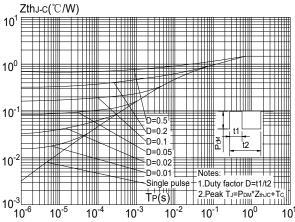


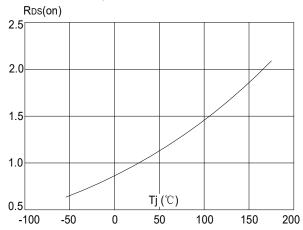
Figure 9: Maximum Safe Operating Area



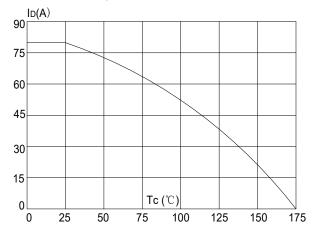
**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Figure 8:** Normalized on Resistance vs. Junction Temperature

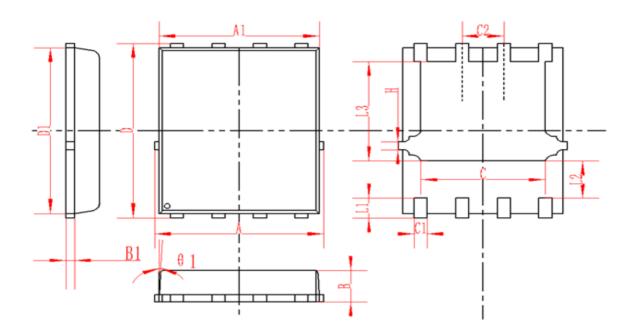


**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



# N-Channel Enhancement Mode MOSFET

# DFN5X6-8L(DFN-8(5.9x5.2)) Package Information



SYMBOL	MM		INCH			
STIVIDOL	MIN	NOM	MAX	MIN	NOM	MAX
А	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
В	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF		0.010REF			
С	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2		1.27TYP			0.5TYP	
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
Н	0.24	0.25	0.26	0.009	0.010	0.010



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