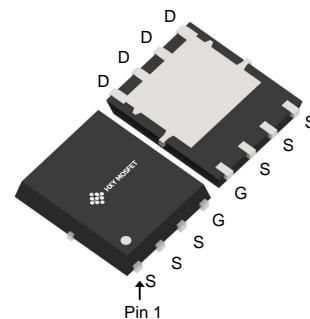




General Description

The FDMS0312AS-NC use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable.

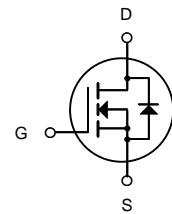


DFN5X6-8L

General Features

$V_{DS} = 30V$ $I_D = 60A$

$R_{DS(ON)} < 5.8m\Omega$ @ $V_{GS} = 10V$



N-Channel MOSFET

Applications

Consumer electronic power supply Motor control

Synchronous-rectification Isolated DC

Synchronous-rectification applications

Ordering Information

Product ID	Pack	Brand	Qty(PCS)
FDMS0312AS-NC	DFN5X6-8L	HXY MOSFET	5000

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	60	A
$I_D @ T_c = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	38	A
I_{DM}	Pulsed Drain Current	135	A
EAS	Single Pulse Avalanche Energy	29.8	mJ
$P_D @ T_c = 25^\circ C$	Total Power Dissipation	30	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JC}$	Thermal Resistance from Junction-to-Ambient	4.6	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	50	$^\circ C/W$



Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\text{uA}$	30	---	---	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=20\text{A}$	---	4.4	5.8	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=15\text{A}$	---	6.9	9	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\text{uA}$	1.2	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=20\text{A}$	---	67	---	S
R_g	Gate Resistance	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=15\text{A}$	---	8	---	nC
Q_{gs}	Gate-Source Charge		---	2.4	---	
Q_{gd}	Gate-Drain Charge		---	3.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\Omega$	---	7.1	---	ns
T_r	Rise Time		---	40	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15	---	
T_f	Fall Time		---	6	---	
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	814	---	pF
C_{oss}	Output Capacitance		---	498	---	
C_{rss}	Reverse Transfer Capacitance		---	41	---	
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	60	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=20\text{A}$, $di/dt=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	15	---	nS
Q_{rr}	Reverse Recovery Charge		---	25	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=24\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Characteristics

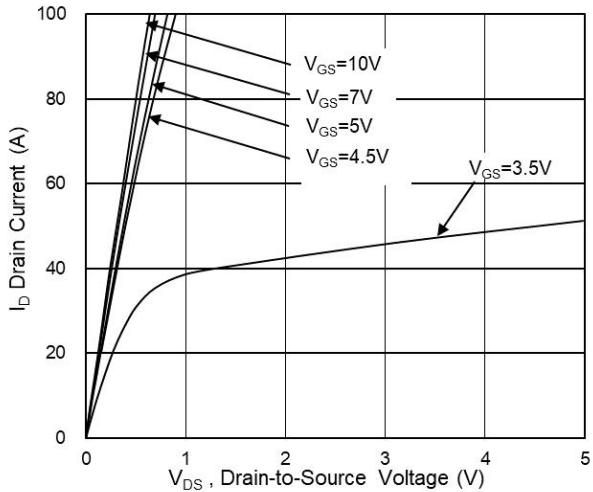


Fig.1 Typical Output Characteristics

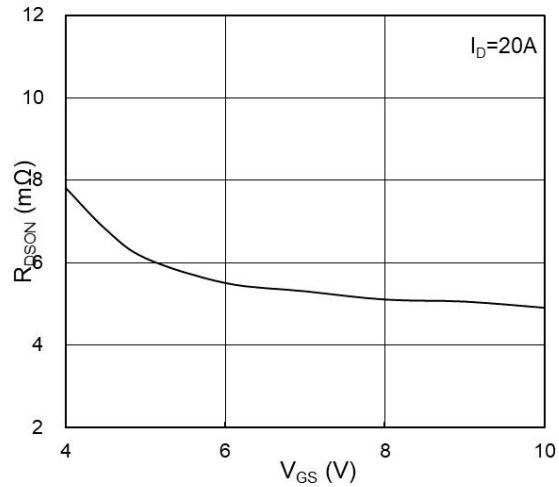


Fig.2 On-Resistance vs G-S Voltage

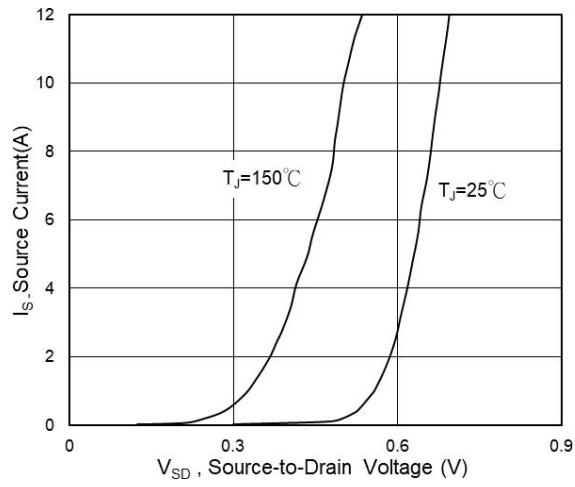


Fig.3 Source Drain Forward Characteristics

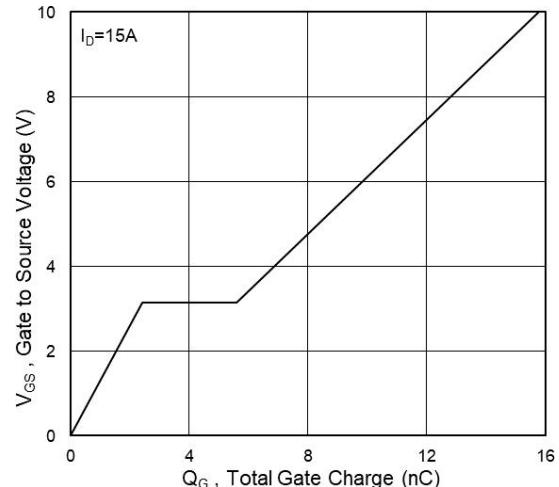


Fig.4 Gate-Charge Characteristics

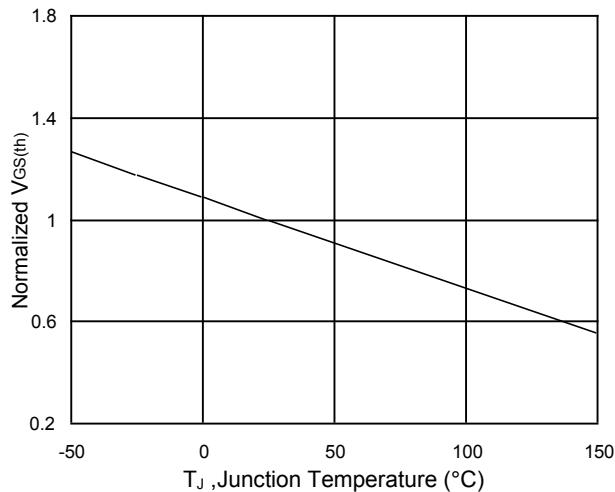


Fig.5 Normalized $V_{GS(th)}$ vs T_J

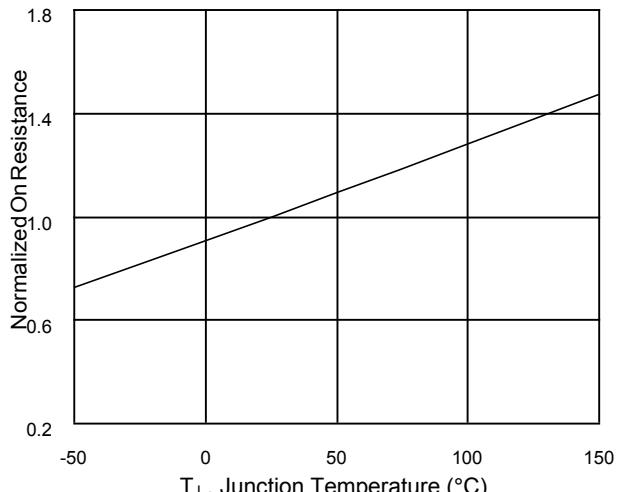


Fig.6 Normalized $R_{DS(on)}$ vs T_J

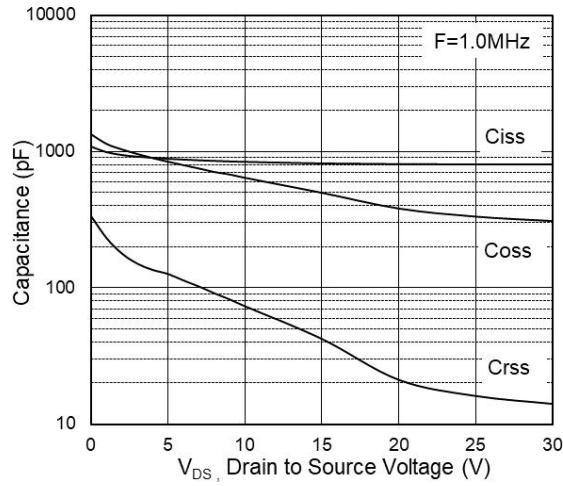


Fig.7 Capacitance

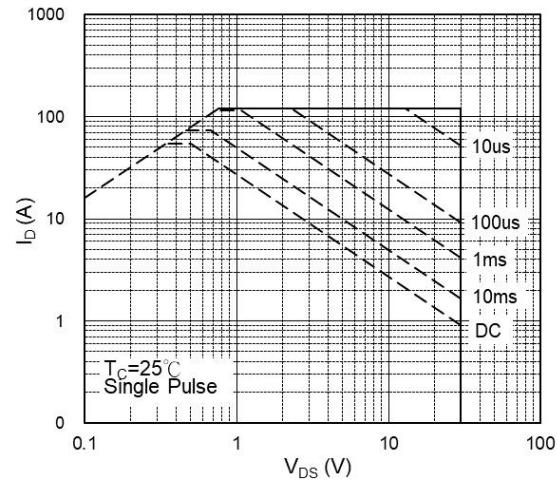


Fig.8 Safe Operating Area

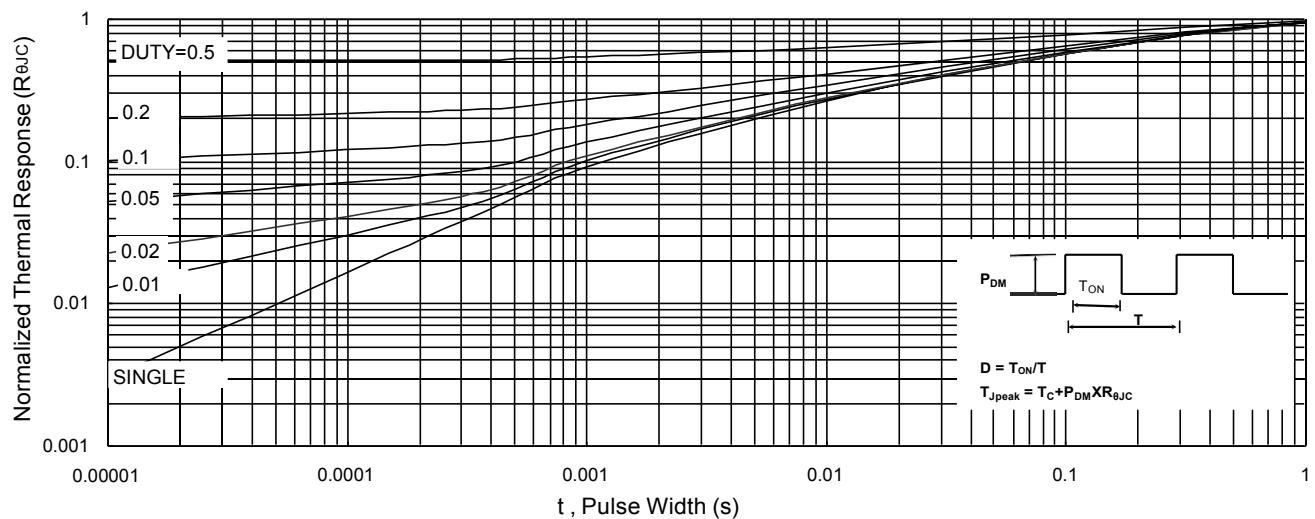


Fig.9 Normalized Maximum Transient Thermal Impedance

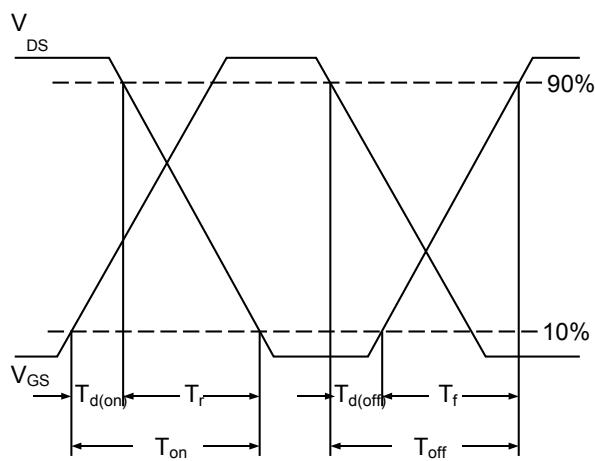


Fig.10 Switching Time Waveform

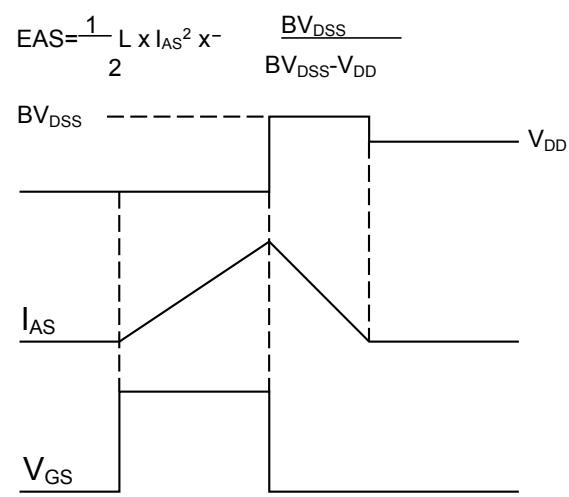
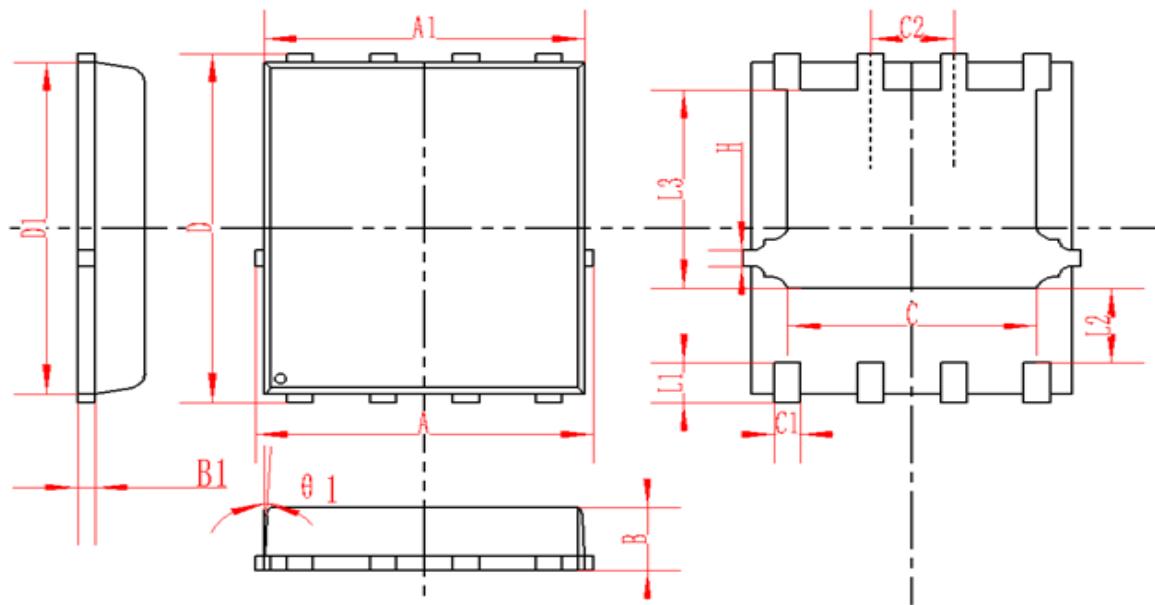


Fig.11 Unclamped Inductive Switching Waveform



DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010



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