



Description

The HXY30P03DF uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is well suited for high current load applications.

General Features

$V_{DS} = -30V, I_D = -30A$

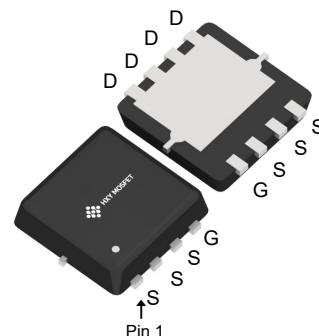
$R_{DS(ON)} < 20m\Omega @ V_{GS} = -10V$

$R_{DS(ON)} < 30m\Omega @ V_{GS} = -6V$

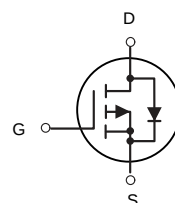
Application

High side switch for full bridge converter

DC/DC converter for LCD display



DFN3X3-8L



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
HXY30P03DF	DFN3X3-8L	40P03 xxxx	5000

Absolute Maximum Ratings@ $T_J = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _A =25°C	Drain Current ³ , V _{GS} @ 10V	-30	A
I _D @T _A =100°C	Drain Current ³ , V _{GS} @ 10V	-15.8	A
I _{DM}	Pulsed Drain Current ¹	-100	A
P _D @T _A =25°C	Total Power Dissipation	22	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C
R _{thj-c}	Maximum Thermal Resistance, Junction-case	5.7	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	79	°C/W



Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Gate-body Leakage current		I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	$T_J=25^{\circ}C$	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μA
	$T_J=100^{\circ}C$			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-2.5	V
Drain-Source On-Resistance ⁴		$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$	-	15	20	m Ω
			$V_{GS} = -4.5V, I_D = -6A$	-	22.5	30	
Forward Transconductance ⁴		g_{fs}	$V_{DS} = -10V, I_D = -10A$	-	23.5	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C_{iss}	$V_{DS} = -15V, V_{GS} = 0V, f = 1MHz$	-	980	-	pF
Output Capacitance		C_{oss}		-	137	-	
Reverse Transfer Capacitance		C_{rss}		-	113	-	
Gate Resistance		R_g	$f = 1MHz$	-	10.5	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q_g	$V_{GS} = -10V, V_{DS} = -15V, I_D = -10A$	-	20	-	nC
Gate-Source Charge		Q_{gs}		-	3	-	
Gate-Drain Charge		Q_{gd}		-	5.5	-	
Turn-On Delay Time		$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -15V, R_G = 3\Omega, I_D = -10A$	-	7.5	-	ns
Rise Time		t_r		-	16	-	
Turn-Off Delay Time		$t_{d(off)}$		-	49	-	
Fall Time		t_f		-	32	-	
Body Diode Reverse Recovery Time		t_{rr}	$I_F = -10A, dI_F/dt = 100A/\mu s$	-	21	-	ns
Body Diode Reverse Recovery Charge		Q_{rr}		-	12.5	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V_{SD}	$I_S = -10A, V_{GS} = 0V$	-	-	-1.2	V
Continuous Source Current	$T_C=25^{\circ}C$	I_S	-	-	-	-30	A

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^{\circ}\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -23A$.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.



Typical Performance Characteristics

Figure1: Output Characteristics

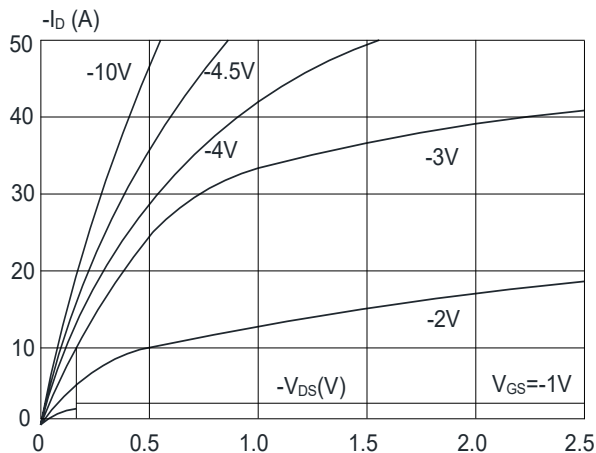


Figure 2: Typical Transfer Characteristics

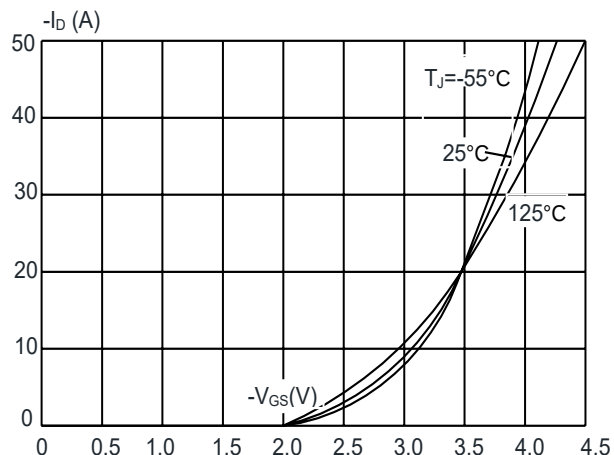


Figure 3: On-resistance vs Drain Current

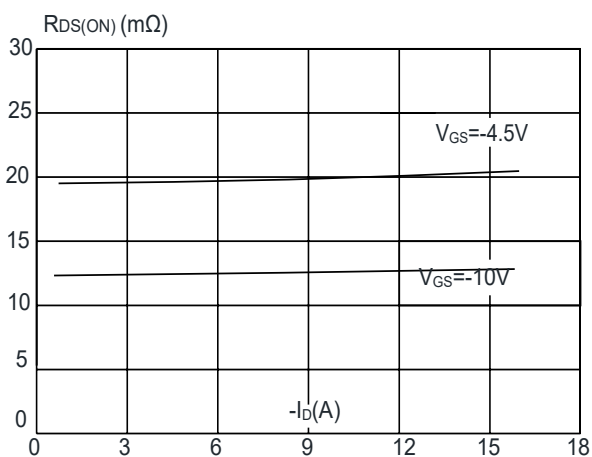


Figure 4: Body Diode Characteristics

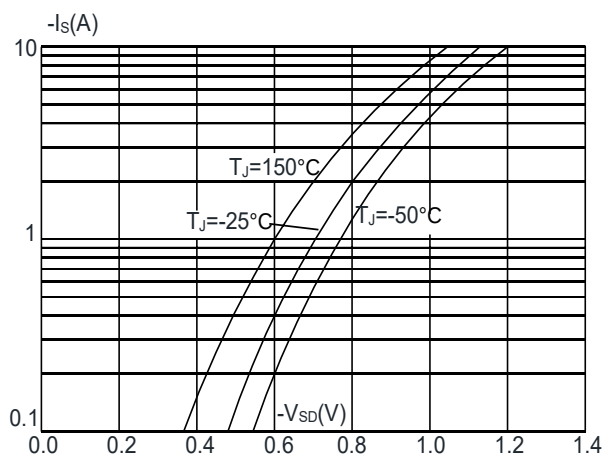


Figure 5: Gate Charge Characteristics

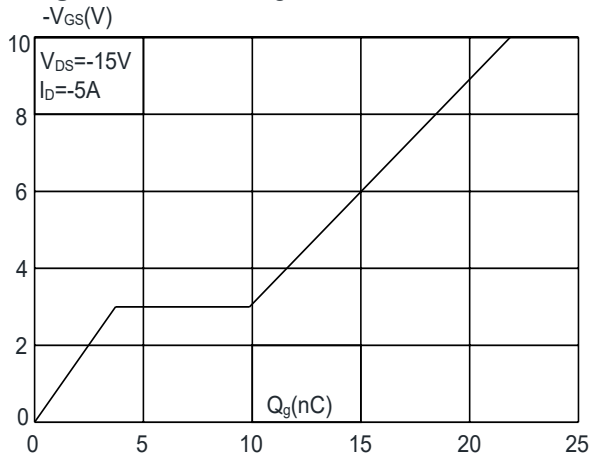
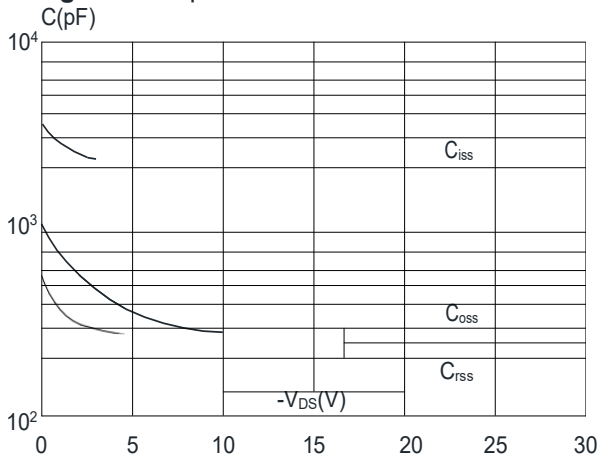


Figure 6: Capacitance Characteristics



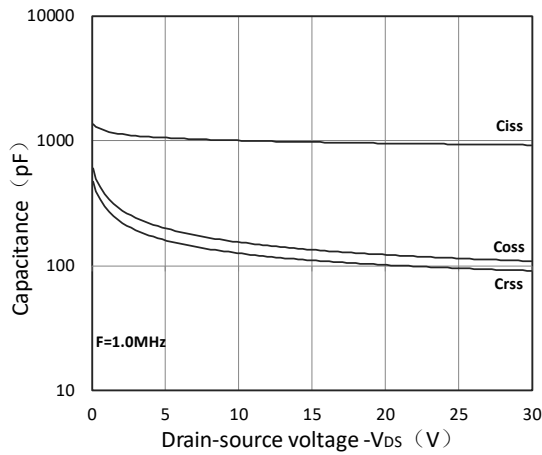


Figure 7. Capacitance Characteristics

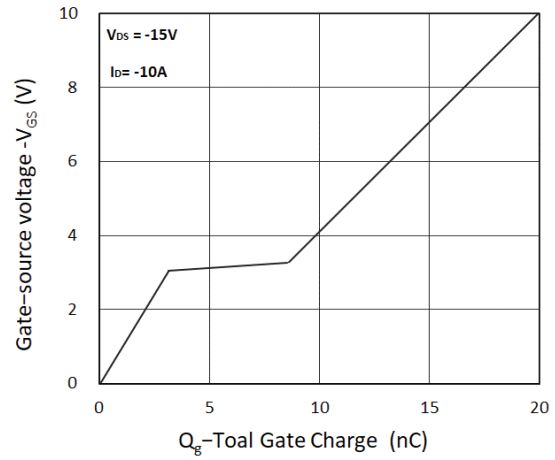


Figure 8. Gate Charge Characteristics

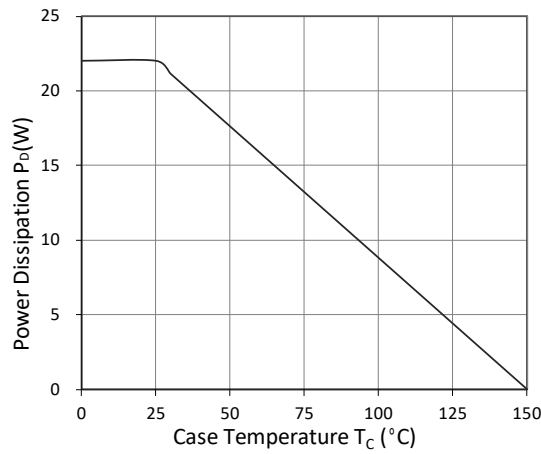


Figure 9. Power Dissipation

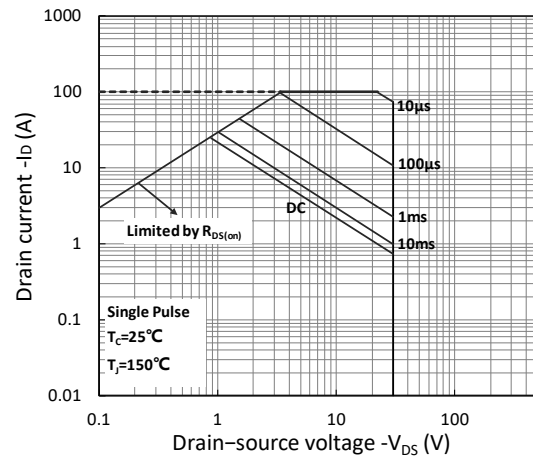


Figure 10. Safe Operating Area

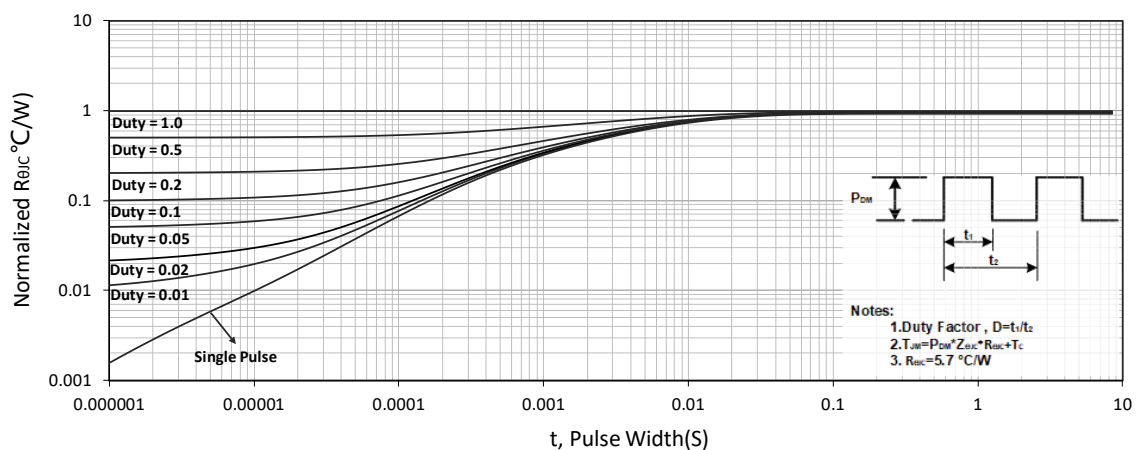
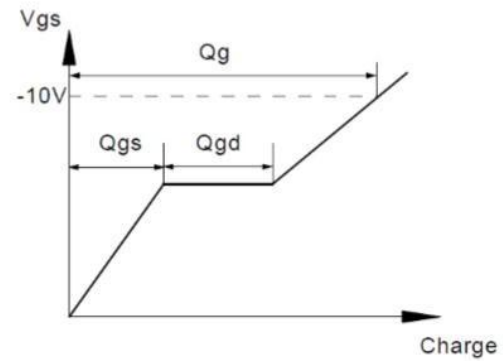
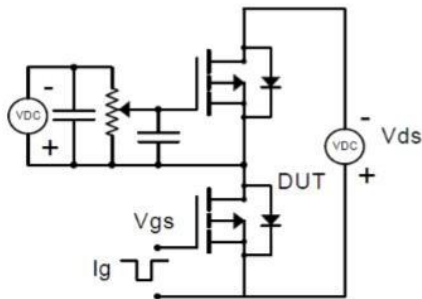


Figure 11. Normalized Maximum Transient Thermal Impedance

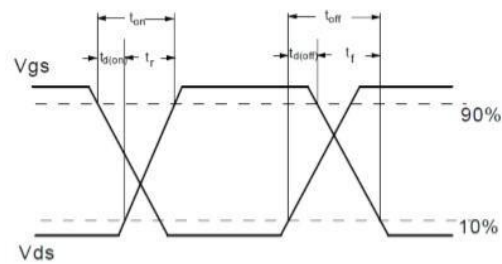
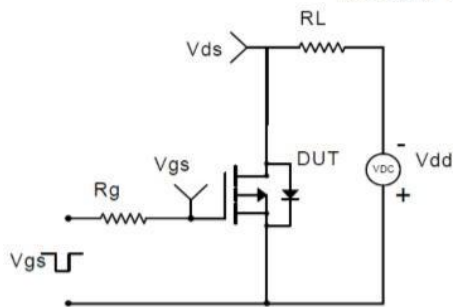


Test Circuit

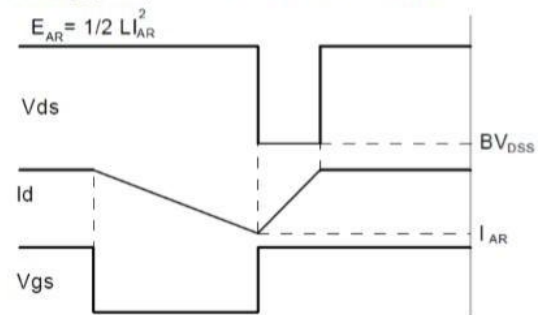
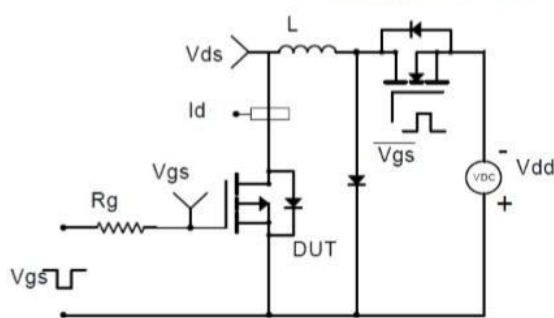
Gate Charge Test Circuit & Waveform



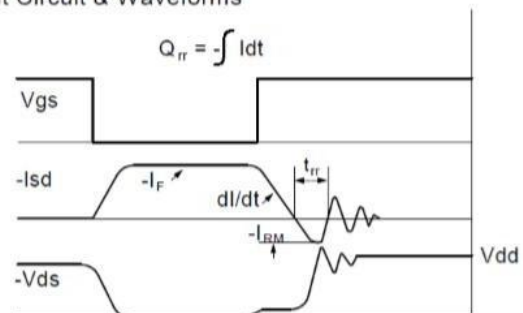
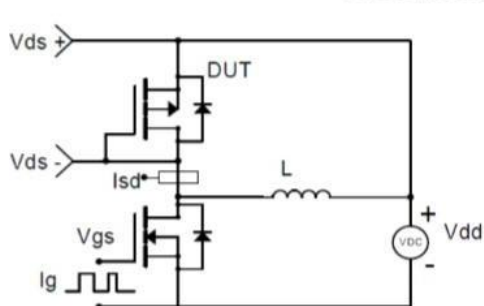
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

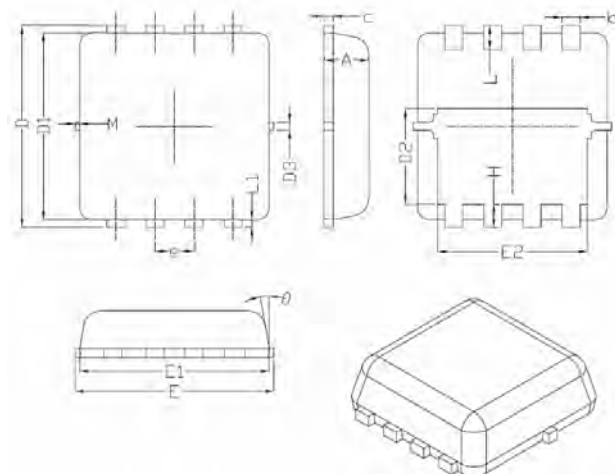


Diode Recovery Test Circuit & Waveforms





DFN3X3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°



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